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OPERATING INSTRUCTIONS

MODEL TTS 58ARP IMPULSE NOISE COUNTER

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MODEL TTS 58ARP IMPULSE NOISE COUNTER

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Issued May 1967
Printed in U.S.A.

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https://archive.org/details/manualsplus_08208

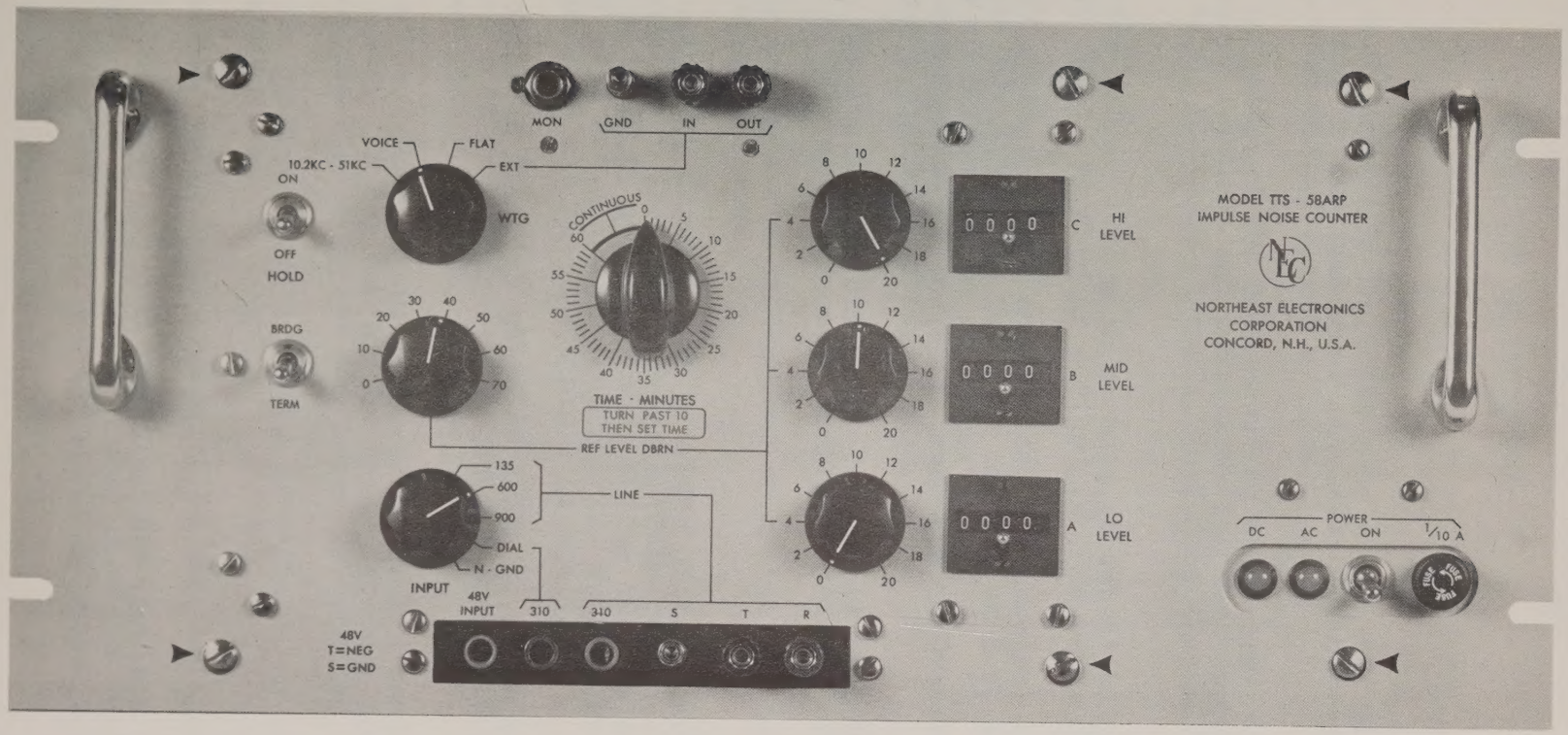

MON
GND
IN
OUT
VOICE
FLAT
EXT
10.2KC - 51KC
ON
OFF
HOLD
WTG
CONTINUOUS
TIME - MINUTES
TURN PAST 10
THEN SET TIME
BRDG
TERM
REF LEVEL DBRN
135
600
900
DIAL
N - GND
LINE
INPUT
48V
INPUT
310
S
T
R
48V
T=NEG
S=GND
C
HI
LEVEL
B
MID
LEVEL
A
LO
LEVEL
MODEL TTS - 58ARP
IMPULSE NOISE COUNTER
NORTHEAST ELECTRONICS
CORPORATION
CONCORD, N.H., U.S.A.
POWER
DC
AC
ON
1/10 A
FUSE

FIG-1

MODEL TTS 58ARP IMPULSE NOISE COUNTER

OPERATING INSTRUCTIONS

1.0 GENERAL

1.01 The TTS 58ARP Impulse Noise Counter is a test set which will count and display the number of impulses exceeding selectable levels over a predetermined length of time.

1.02 The unit is designed for rack mounting and contains all of the necessary features and provisions for many impulse noise tests on audio lines and data channels, including the 40.8 kilobit systems.

1.03 It is calibrated in dbrn with a range of sensitivity from 0 dbrn to 90 dbrn. 90 dbrn is defined as .775 volts RMS.

1.04 The count is displayed on three electro-mechanical counters. Sensitivity is adjustable for each counter in 2 db steps with a maximum of 20 db difference in the three channels. The three counters allow examination of the noise spectrum in discrete amplitude steps giving a histogram presentation.

1.05 It allows termination or bridging of circuits on 600 ohms, 900 ohms, or 135 ohms. Input circuits are highly balanced.

1.06 Provisions are made for dialing out on a line and holding the circuit established.

1.07 Internal weighting networks are provided which produce a FLAT response over the audio range, a VOICE response which simulates C-MSG weighting, and 10.2 to 51 KC for 40.8 kilobit data systems. An EXT position allows use of special weightings when necessary. Figures 15 and 16 show typical responses.

1.08 The unit operates from 115 volts AC ±10%, 47 Hz to 63 Hz, or 48 volts station battery. The general description of the 115 volt AC power supply is given in Appendix A.

1.09 A spring driven timer allows measurement over a predetermined length of time. At the end of the timed interval power is disconnected from the circuitry and the count is retained.

1.10 A monitor is provided for listening to noise as an aid in identification.

1.11 Noise to ground measurement capabilities are included.

1.12 The unit is designed for rack mounting and requires 8 3/4" of panel height in a standard 19" relay rack and weighs 16 pounds complete with protective rear cover and AC power supply.

2.0 CIRCUIT DESCRIPTION

2.01 The unit consists of the following sections which will be treated individually: Input, Amplifier 1, Amplifier 2, Attenuators, Filter, Channel Amplifier and Phase Splitter, Flip Flops, Gates, Timing, Counter Driver, Power, and Monitor. References are made to the appropriate figures. The interconnection of these circuits is shown in the block diagram, Figure 2.

Input (Figure 3)

2.02 The line is connected to the circuitry through a balancing transformer, T1. This is DC blocked (up to 150 volts) by C1 and C2. These electrolytics are effectively back to back, so one will be polarized correctly no matter which polarity DC appears on the line.

2.03 When a terminated input is chosen by the TERM/BRDG switch, a resistive load is applied to the line side of the transformer. The value of this load is determined by INPUT switch S1 to be 600, 900, or 135 ohms. S1 also selects the proper turns ratio so that no correction is necessary on changing impedance.

2.04 For line holding, a low resistance (approximately 500 ohms) holding coil can be applied directly across the LINE by means of the HOLD switch. This is independent of the INPUT switch.

2.05 To obtain a line, the INPUT switch has a DIAL position which connects the LINE connections to the DIAL jack.

2.06 To measure noise to ground (NGND) the components of noise from each line are added in a summing circuit. The sum is then connected to the REF LEVEL attenuator.

2.07 Connections from the line to the set are by binding posts (on 3/4" centers to accept GR274 type connectors) or a 310 type plug.

Amplifier 1 (Figure 4)

2.08 This is a four stage amplifier (including two emitter followers) which has about 36 db of gain. Negative feedback is incorporated to stabilize the gain.

2.09 Q1 is an emitter follower which isolates the attenuator from the amplifier.

2.10 Q2 and Q3 are common emitter amplifiers. Q4 is an emitter follower output to isolate the filters. The negative feedback is taken from the emitter of Q4 and applied to the emitter of Q2.

Amplifier 2 (Figure 4)

2.11 This is a three stage amplifier (including an emitter follower) which has about 35 db of gain. Negative feedback is incorporated (from the emitter of Q7 to the emitter of Q5) to stabilize the gain.

2.12 The feedback is, in part, determined by TH1, a thermistor whose resistance will change with temperature. This produces a small temperature compensation to offset effects of other circuits. As the temperature increases, the resistance of TH1 will decrease, the negative feedback will increase, and the gain of Amplifier 2 will decrease.

2.13 Q5 and Q6 are conventional common emitter stages.

Filters (Weighting Networks) Figures 4, 15, and 16

2.14 The networks to produce weighting for 10.2 to 51 KC and VOICE are cascaded high pass, low pass filters of a constant K configuration.

2.15 For the 10.2 to 51 KC network, C10, L2, and C11 form a T section high pass, while C12, L3, and C13 form a Pi section low pass. The combination produces a bandpass as shown in the response curves. C14, L4, C15, C16, L5,and C17 comprise similar sections for VOICE WTG.

2.16 For the FLAT WTG shunt capacity is added (C18) to restrict the bandwidth to the normal range.

2.17 Since the insertion loss of these filters may not be identical, the loss is equalized at S5.2A so that no correction need be applied when using the various internal weightings. On using the external weighting, a network having an insertion loss of two db should be used, otherwise the overall sensitivity of the set, including the external weighting, will not be that indicated by the REF LEVEL switches.

2.18 The impedance for the networks, either internal or external, is 600 ohms, both source and load. The source impedance is determined by R27, which builds out the output impedance of Amplifier 1 to be 600 ohms. The load impedance for the networks is 600 ohms resistive, the series combination of R27, R28, and R29.

Attenuators (Figures 3 and 4)

2.19 A total of 70 db is common to all three channels. This is controlled by S4, the REF LEVEL DBRN switch, with 10 db steps 0 to 70.

2.20 This attenuation is before and after Amplifier 1 in the following manner: The first two attenuator positions (10 and

20 DBRN) add 10 db per position (10 and 20 db attenuation) after Amplifier 1. This loss is on S4.4A (Figure 4) and is an L type pad consisting of R27, R28, and R29. This loss (20 db) remains in the circuit for all other positions (30 to 70 DBRN) of S4, and 10 db step attenuator.

2.21 Another L type pad is on S4.3A (Figure 3), and consists of R11, R12, and R10. With S4 on 30 DBRN, 10 db of this pad is inserted ahead of Amplifier 1. Remember that S4.4A inserts 20 db in this and higher positions after Amplifier 1.

2.22 When S4 is switched to 50 DBRN, the pad on S4.3A produces no attenuation. Instead, another pad consisting of 30 db is inserted. This pad consists of R8 and R9 (Figure 3). The 50 db of attenuation then consists of 30 db due to R8 and R9 ahead of Amplifier 1, plus the 20 db on S4.4A after Amplifier 1.

2.23 When S4 is switched above 50 DBRN (60 and 70) the pad on S4.3A once again is used to add 10 db and 20 db of attenuation.

2.24 Each channel also has 20 db of individual control in 2 db steps. This is shown, for the LO LEVEL channel, on S6 (Figure 4). It is a series string consisting of R101 through R110 driving resistors R111 and R112. (R111 is an internal calibration adjustment for this channel.)

2.25 The 20 db in 2 db steps is repeated in an identical fashion (except for symbol numbers) for the other two channels.

Channel Amplifier and Phase Splitter (Figure 5)

2.26 After the signal is passed through Amplifier 1 and Amplifier 2 weighted by the appropriate network and set in level by the attenuators, it branches into three identical channels designated by LO, MID, and HI LEVEL. The description here and the schematic generally refer to the LO LEVEL, but similar descriptions and schematics would apply for the other two.

2.27 The output of the 2 db attenuator is given some amplification by Q101, a common emitter amplifier with emitter degeneration. This amplified signal is then fed to the base of Q102, which operates as a phase splitter.

2.28 The collector of Q102 delivers a negative signal through CR101 and CR105 (positive signals are blocked by these diodes). The emitter of Q102 also delivers a negative signal, this being through CR102 and CR105. (CR103 and CR104 are used to drain C104 and C105 or accumulated charge.)

2.29 To understand the operation of this, imagine that the signal delivered to the base of Q102 is an impulse which has a negative peak followed by a positive peak.

2.30 The negative peak will cause Q102 to increase conduction. This means that the emitter will go in a negative direction and the collector will go in a positive direction. The negative going emitter voltage allows conduction of CR102 and CR105, and this negative signal is passed. The positive going collector signal is blocked from subsequent circuitry by CR101.

2.31 Thus, when the base of Q102 goes negative, CR105 conducts and passes a negative signal.

2.32 Later, when the base of Q102 goes positive, the transistor will decrease conduction, the emitter follows the base in a positive going voltage, less negative, while the collector goes more negative. The positive going signal at the emitter is blocked by CR102. The negative going signal at the collector is passed through CR101 and CR105.

2.33 Thus, when the base of Q102 goes either positive or negative, a negative output will be available from CR105.

Flip Flop (Figure 5)

2.34 This is a bistable SET/RESET multivibrator consisting of Q103 and Q104. In the reset mode, Q104 is normally ON and Q103 is normally OFF. It is held in this state by the cross coupled bias arrangement. With Q103 OFF, its collector is highly negative, which supplies heavy bias through R130 to Q104. Q104 is held ON, its collector saturates, leaving little voltage. Since this voltage is the bias supply for Q103, essentially no base current is available for Q103 and it is held OFF.

2.35 When CR105 conducts, at sufficient level, base current flows into Q103. This produces collector current in Q103, lowers its collector voltage, lowers the bias for Q104, which tends to cut off. This raises the collector voltage of Q104 and supplies more base current for Q103. This aids the signal from CR105. The operation described above is regenerative, and when a signal appears out of CR105 at a sufficient amplitude, Q103 is turned ON and Q104 is turned OFF. This is also a stable state and will remain there until reset. Note that further signals from CR105 will now have no effect since Q103 is already ON as hard as it can be and signals from CR105 must be negative, which only try to turn Q103 on harder.

2.36 In summary, if a sufficient signal is passed by CR105, the multivibrator will flip into the SET condition and stay there until reset.

Gates (Figures 5 and 6)

2.37 A typical gate is shown in Figure 5. It consists of R135, CR108, CR109, CR110, and CR111. The anode of each diode is connected to a collector of a transistor. Typical interconnections,

in an abbreviated manner, are shown in Figure 6. Let us first consider the gate which leads to Q105, the LO LEVEL channel.

2.38 The four diodes are connected to four different collectors. CR108 is connected to the normally ON transistor of the LO LEVEL. CR109 goes to the normally OFF of the MID LEVEL. CR110 goes to the normally OFF of the HI LEVEL, and CR111 goes to the normally ON transistor of the TIMING multivibrator described in paragraph 2.45, 2.46, 2.47.

2.39 When a diode is connected to an ON transistor, the anode is returned to a voltage near ground, since in all of this discussion, when a stage is designated ON, it is considered fully conducting with essentially no voltage at the collector, and when OFF, fully off with essentially full battery voltage at the collector.

2.40 When the anode is at or near ground, the diode will conduct, since the cathode is returned to a negative supply. When conducting, the cathode will be slightly negative, but still near ground, the battery voltage being developed in this case across R135. If any of the four diodes are returned to an ON transistor, that diode (or diodes) will conduct and the voltage at the output (the junction of the four diodes) will be essentially zero. It does not matter how many diodes conduct as long as there is at least one.

2.41 It is only when all four transistors are OFF simultaneously that an output is produced. Under this condition all four anodes will be connected to highly negative voltages (OFF transistors). The diodes cannot conduct unless the cathodes are negative in respect to the anodes. There is no current in R135. The gate output rises to a negative value.

2.42 Each of the three gates has four inputs. Of these, one input for all gates is common and is connected to the TIMING MONO. This input has nothing to do with amplitude, but is used as a strobe, or clock, pulse.

2.43 The other three inputs contain information as to whether the pulse is of an amplitude to trigger the LOW, MID, or HI LEVEL. Remember that the sensitivities are such that the LO is first to be triggered. If the impulse is large enough to flip the MID LEVEL SET/RESET, then it must also be more than large enough to flip the LO LEVEL. Further, if the HI LEVEL is triggered, all three channels will be triggered.

2.44 Figure 6 contains a Truth Table which indicates which conditions are necessary to produce outputs from the three gates.

Counter Driver (Figure 5)

2.45 A typical circuit is shown in Figure 5 for Channel A (LO LEVEL).

This is duplicated for the other two channels. When the gate produces an output, a highly negative pulse is applied to C110 and the base of Q105. The capacitor charges, and this charging current turns Q105 on hard. The collector current of Q105 is available as base current for Q106 (note that these are opposite polarity transistors) which is also turned on hard and provides considerable current into the counter winding.

2.46 This winding is dependent on C110 charging, and when this ceases the output current will also cease.

2.47 When a channel is triggered, the associated counter will be driven by a pulse of current.

Timing (Figure 7)

2.48 The maximum count rate is eventually limited by the counter. The current wave into the solenoid must be pulsed on long enough for it to energize and must be removed long enough to de-energize, both functions being necessary to produce a count. To guarantee that such conditions will be produced, no matter at what rate or interval the impulses occur, timing circuits are incorporated. Two timed intervals are provided and are produced by the circuits labeled TIMING MONO and RESET MONO.

2.49 The TIMING MONO consists of Q401 and Q402 arranged in a monostable multivibrator configuration. The stable state is with Q401 OFF and Q402 ON, since Q402 gets its bias from battery (through R406), while Q401 gets its bias from the collector of Q402 (through R408).

2.50 When a negative pulse is applied to Q401, this side will go on. The positive going (from negative battery to ground) pulse at the collector of Q401 is coupled by C402 to the base of Q402, where it appears as a positive voltage and turns off Q402. The collector of Q402 goes to battery and supplies bias to Q401 to hold that side on even after the trigger pulse is removed. Q402 will stay off as long as its base is biased off. C402 immediately begins to discharge through R406. The rate of discharge depends on the value of C402 and C406 (among other things). After a given length of time C402 will not only be discharged, but will tend to recharge in the opposite direction. However, this drives the base of Q402 sufficiently negative so that it conducts, after which the circuit regeneratively reverts back to the original stable state.

Reset (Figure 7)

2.51 The RESET MONO is a monostable multivibrator consisting of Q403 and Q404. Its operation is similar to that of the TIMING MONO described in the Timing section. The RESET MONO is triggered from Q401 through CR403. This occurs at the end of the TIMING pulse. The time interval corresponding to when this circuit is timing (in its semi-stable state with Q403 ON and Q404 OFF) is dead

time. The gates produce no output. The SET/RESETS are as placed earlier, and this dead time is used to allow the mechanical counter ample time to de-energize and complete the count, and for C110 to discharge. At the end of the RESET interval (about 60 msecs) a reset pulse is produced and fed to each SET/RESET mono, which is then capable of recognizing further impulses.

Power (Figures 3 and 7)

2.52 The main power for the set is derived from 115 volts AC (see Appendix A) or an externally supplied 48 volt DC source. The 48 volts is dropped to 18 volts through R42 and R42A and CR1 (Figure 3). Polarity protection is achieved by CR1. With improper polarity applied, this diode does not conduct and prevents damage to the circuitry.

2.53 The 18 volt (B1) point is further dropped to 12 volts (B2) (Q405 and associated circuits) and 9 volts (B3) (Q406 and associated circuits). These are shown in Figure 7.

2.54 The 18 volt supply is controlled by the TIME and POWER switches. Note that at the end of a timed interval, with TIME at the OFF position, the 18 volts is automatically disconnected from the circuit, but there will still be a current drain from the 48 volt supply.

2.55 When operating from external 48 volts, the insertion of the plug into the 48 volt jack automatically disconnects the internal power supply.

CAUTION: When using an external 48 volts, always make the connection to the TTS 58ARP first, then connect to the 48 volts. When disconnecting, always disconnect from the 48 volt buss first. Failure to do so can result in a momentary short if the TTS 58ARP is grounded.

Monitor (Figure 4)

2.56 A portion of the signal out of Amplifier 2 is fed to the monitor amplifier, Q8. This stage provides amplification and isolation of the circuitry from the headphone or other device connected to the MON jack.

2.57 The level at the MON jack is controllable by the 10 db step attenuator. The three 2 db step attenuators are after this point, and thus cannot influence the level at the monitor output.

2.58 The MON jack has approximately 600 ohms output impedance and will deliver a level equivalent to nearly -22 dbm into a 600 ohm load when the sensitivity is such that Channel A just counts when its 2 db step attenuator is on the 0 position.

2.59 The power to the monitor amplifier is controlled by the MON jack (as well as the TIME switch). When the monitor is not used, it draws no power.

CAUTION: Inserting or withdrawing a plug from the MON jack may produce an additional count on any register.

3.0 CONTROLS AND TERMINALS

3.01 Lower Jack Strip

a. 48V - connections to the set when using external 48 volt battery. This accepts a 310 type plug with tip negative and sleeve ground.

b. DIAL 310 - a jack to accept a 310 type plug to allow an external dial to be used.

c. LINE 310 - a jack to accept a 310 type plug to allow connection to the line to be tested.

d. LINE S-T-R - binding posts which connect to sleeve, tip, and ring of the LINE 310.

3.02 INPUT - a five position rotary switch which selects the LINE impedance to be 600, 900, or 135 ohms, or connects the LINE jack to the DIAL jack, or selects noise to ground (N-GND).

3.03 POWER - controls power to the set.

3.04 BRDG/TERM - a toggle switch which terminates the LINE in an impedance selected by the INPUT switch or bridges across such an impedance.

3.05 HOLD - a toggle switch which, when ON, connects a low resistance holding coil across the LINE. When OFF, the input connection is blocked up to 150 volts DC.

3.06 WTG - a four position switch which selects the frequency response of the set.

a. 10.2-51 KC - passes this band (±1 db) and attenuates below and above this band. It is meant to be used in the 40.8 kilobit data systems.

b. VOICE - simulates a C-MSG weighting.

c. FLAT - has a flat response over the audio range, 3 db at approximately 40 cps and 10 Kcps.

d. EXT - allows connection of an external weighting network to the indicated binding posts. This external network should be a 600 ohm device and have two db loss. Other losses can be used with suitable corrections to the indicated sensitivities.

3.07 TIME-MINUTES - a spring driven timer which, when turned clockwise, turns on the power to the set for the indicated time.

A continuous position (ccw) gives an untimed position which must be manually terminated.

3.08 REF LEVEL DBRN

a. 0-70 an eight position switch which varies the sensitivity of all three counters simultaneously in 10 db steps.

b. 0-20 - three eleven position switches. Each switch is associated with one counter and varies the sensitivity of that counter (and only that counter) in two db steps.

c. The sensitivity of each counter is the sum of the main setting (0-70) and its own associated attenuator (0-20).

3.09 Counter Registers - three electromechanical counters, each having four digits and each being manually reset to zero.

3.10 Upper Jack and Terminal Group

a. MON - accepts a 310 type jack with connections to tip (signal) and a common sleeve and ring (chassis) for monitoring with a headset.

b. GND-IN-OUT - associated with the EXT position of the WTG switch. Allows connection of an external weighting network (see 3.06 d). IN and OUT are spaced to accept a GR274 type connector. The GND connector connects to chassis and circuit common. It is used to ground the set independently of the use of the WTG switch.

4.0 OPERATION

4.01 Connect an AC cord to the 115 volt AC line. Turn the POWER switch to ON. The AC lamp will light.

4.02 Turn the timer knob clockwise, a click will be heard, and the DC lamp will light.

4.03 Connect to the LINE by establishing a connection to either the 310 jack or the T and R binding posts (the T and R binding posts are spaced to accept a twin banana plug similar to the GR274).

4.04 Dial the Connection

a. When a connection is to be made which requires dialing connect the dial or phone to the jack marked 310 associated with the DIAL position of the INPUT switch.

b. Place the INPUT switch in the DIAL position and the HOLD switch on OFF.

c. Dial the desired number.

d. Place the HOLD switch in the ON position.

e. The dial can now be removed and the circuit maintained by the HOLD switch.

4.05 Set the INPUT switch to the proper impedance.

4.06 Set the BRDG/TERM switch for either termination or bridging.

4.07 Set the WTG switch to give the desired weighting characteristic. If placed on EXT, an external network must be connected to the associated binding posts. See paragraph 4.15.

4.08 Set Sensitivity

a. The sensitivities of the three channels are the sum of the 10 db step attenuator (0-70) in each case, and the 2 db step attenuator (0-20) of that associated with the counter.

CAUTION: When using the instrument at or near full sensitivity (10 db step on 0 dbrn or 10 dbrn), certain comments and precautions are in order. The monitor leads (if used) should not be draped close to the input leads. The set should not be operated in a strong AC magnetic environment. This is especially true with the HOLD coil in the ON position. (It is strongly advised

that the HOLD coil be in the OFF position at these sensitivities.) Accuracy of the set at these positions may be degraded in the FLAT position.

b. The sensitivities of the counters must be set in the proper relationship to each other. The LO LEVEL (A) counter must have the highest sensitivity so that it will respond to the lowest level impulse (lowest dbrn). The HI LEVEL (C) counter must have the lowest sensitivity so that it will respond to the highest level impulse (highest dbrn). The MID LEVEL must be between the other two.

c. When set properly, counter A will register those impulses which exceed the level indicated for A, and are less than indicated for B.

d. B counter will register those counts which exceed that indicated for B and are less than that for C.

e. C counter will register all counts which exceed that indicated for C.

f. Example 1

Main (0-7) REF LEVEL setting on 40
A on 0
B on 6
C on 12
A has 156 counts.
B has 68 counts
C has 7 counts

This indicates -

156 counts were greater than 40 dbrn but less than 46 dbrn.

68 counts exceeded 46 dbrn but were less than 52 dbrn, and 224 (156 + 68) counts exceeded 40 dbrn but were less than 52 dbrn.

7 counts exceeded 52 dbrn, 75 (68 + 7) exceeded 46 dbrn, and 231 (156 + 68 + 7) exceeded 40 dbrn.

g. Example 2

Main (0-70) REF LEVEL on 30
A on 2
B on 8
C on 16
A has 200 counts
B has 50 counts
C has 10 counts

This indicates -

200 counts exceeded 32 dbrn (30 + 2) but were less than 38 dbrn (30 + 8).

50 counts exceeded 38 dbrn but were less than 46 dbrn (30 + 16).

10 counts exceeded 46 dbrn, 60 were over 38 dbrn, and 260 were over 32 dbrn.

4.09 Set TIMER to the indicated time duration. POWER switch must be ON.

a. This is normally for either 15 or 30 minutes.

b. To set for 30 minute test, rotate the TIMER knob until it is aligned with 30.

NOTE: There is a built-in 20 to 30 second delay after the timer is set and before a register will count.

c. When turned clockwise, a click will be heard which indicates the power is applied.

d. When turned clockwise and released, the timing operation will begin and will be indicated by an audible ticking.

NOTE: The ticking can also be felt when a finger is lightly laid on the TIMER knob.

e. Timing can be changed any time by simply resetting the knob. When released, the set will operate for the time so indicated.

f. Operation can be ended manually by turning knob counter clockwise to 0 MIN and noting a click. Do not turn past 0 into continuous region if set is to be turned off.

g. To operate set manually (untimed), turn TIMER counter clockwise until click is heard into the continuous region.

h. To terminate test when in continuous position, rotate TIMER clockwise toward 0 until click is heard.

i. To set for times of 10 minutes or less, rotate TIMER knob clockwise well past 10 (say to 20) then counter clockwise to desired time.

NOTE: Operation listed above in step 4.09 i is to give long life to the contacts of the timer. Turning

past ten provides spring tension to snap open the contacts at the end of the time.

4.10 Reset All Counters

a. This is done by depressing the small button below the individual displays.

b. This resetting of the counters should be the last thing performed before the start of the test.

4.11 To Use External 48 Volts

a. Insert a 310 type plug-ended cord into the jack marked 48V.

b. Connect the other end of this cord into any convenient station battery outlet.

c. Connections at the TTS 58ARP are negative to tip, positive to sleeve and chassis. (No damage to the set will occur if polarity is reversed, but the set will not operate.)

CAUTION: When connecting external 48 volts to the set, always make connections to the TTS 58ARP first, then to the 48 volt appearance.

d. When a plug is inserted into the TTS 58ARP 48 volt jack, the self-contained power supply is automatically disconnected.

e. The TIMING switch will still control power to the circuitry and automatically terminate the test, but a power drain of approximately 150 ma will be continuously placed on the station battery independent of the TIMING control.

4.12 To Monitor

a. Plug into the MON jack. This accepts a 310 type plug with chassis made to ring and sleeve and signal made to tip.

b. Output is DC blocked (external voltages exceeding 10 volts should not be applied to the MON jack).

c. Monitor level is determined by the 10 db step control (0-70 REF LEVEL) but NOT the 2 db step controls.

d. Response is determined by the WTG switch.

e. Monitor has 600 ohm output impedance but can drive all common type headsets.

f. Monitor level (at input level to produce counting on

Channel A when its 2 db step attenuator is on 0 db) is approximately .2 volts peak into a high impedance.

g. Monitor can be used to drive headphone, CRO, and other devices.

h. At high sensitivities care should be taken to physically separate the monitor leads from the input leads or use shielded cable.

4.13 To Calibrate Set

a. To check the calibration it is necessary to have a signal source whose amplitude is accurately known.

b. A milliwatt supply through an accurate attenuator is normally a convenient source of calibrating voltage.

c. Set INPUT to 600 or 900 ohms to match the signal source.

d. Unless an accurate termination is provided elsewhere, place TERM/BRDG to TERM.

e. Set WTG to VOICE.

f. Set HOLD to OFF.

g. Set POWER to ON.

h. Set main REF LEVEL to 50.

i. Set individual REF LEVELS to:

A	0
B	10
C	20

j. Turn TIMER clockwise. Allow 30 seconds for the normal delay in the TTS 58ARP.

k. Feed in a signal at 1000 cps at a level of -43 dbm. Channel A should be counting. If it is not, increase the level of the input in .1 db steps until it does. This should be within .2 db of -43 dbm. If it was counting at -43 dbm, decrease the level until it stops. The lower level at which counting occurs should be within .2 db of -43 dbm.

l. If Channel A does not count at -43 dbm, ±.2 db, turn R111 counter clockwise, feed in exactly -43 dbm, and advance R111 clockwise until counting just occurs.

m. With Channel A at proper calibration, feed in a level of -33 dbm and check the sensitivity of Channel B in a similar manner. It should begin to count at an input level of -33 dbm, ±.2. If not, adjust R211 for proper sensitivity with an input of -33 dbm.

n. Channel C is checked or adjusted in the same manner with -23 dbm as the nominal level and R311 as the adjustment.

NOTE: Using a sine wave to calibrate the set, it may be noticed that the count rate changes with input level. At threshold the counters may only register once per second or be irregular in their rate. When the input level is raised, the rate becomes regular although at this point it may be less than 10 per second. At higher level inputs the full 10 per second will be observed. All of this is somewhat normal. The spread between barely counting and counting at full speed is normally less than .3 db. The customary method used to define threshold is that level required to produce a steady, rhythmic counting rate independent of speed. The limits stated above are for normal room ambient temperatures. At temperatures other than this, sensitivity may vary more than ±.2 db.

o. A pulse can be used to calibrate the set. All of the previous instructions will apply if a pulse source having 600 ohm output impedance and 1.55 volts peak amplitude into an open circuit is available. This pulse can be of either polarity and almost any shape. The two sources of calibrating voltage (sine or pulse) will yield results within .5 db.

4.14 To Measure Steady Noise

a. Although not intended for this type measurement, approximate results may be obtained when no other instrument is available.

b. Because this instrument measures peak amplitude while noise (steady) measurements are made on a basis other than peak, and since the definition of REF LEVEL is different, a correction must be applied.

c. The correction that must be applied depends somewhat on the noise being measured.

d. For normal "white" noise the approximate correction is 13 ±2 db when comparing VOICE setting to C-MSG or FLAT to FLAT 15 KC.

e. To measure steady noise connect to the circuit as described in preceding paragraphs.

f. Set B and C Channel attenuators at 20 db. Set A at 0 db.

g. Set REF LEVEL (10 db steps) at the lowest number for which continuous rapid counting occurs on Channel A.

h. Advance Channel A attenuator in 2 db steps until the count becomes slow and erratic (less than one per second) or ceases.

i. Decrease the setting 2 db and the count should exceed one per second. Note the sum of this reading and the 10 db attenuator (step g).

j. Use the monitor to identify the signal as either "white" noise (the rushing sound of a radio not tuned to a station), power induction, or tone.

k. For white noise apply the correction of step 4.14 d. This correction is subtracted from the dial settings of steps g and i.

EXAMPLE: Step g results in a setting of 30 and step i in a setting of 8, or a reading of 38 dbrn. Noise sounds white, WTG is VOICE. The approximate steady noise is 38-13 or 25 dbrn C.

l. For tone or power induction the correction is less and depends on the amount of tone or induction and noise. If all tone (no noise) a 3 db correction is applied.

4.15 To Use an External Filter

a. Filter should be for 600 ohms and have a 2 db insertion loss.

b. If filter is at an impedance other than 600 it must be:

1. Built out to be 600 ohms and the resulting insertion loss determined and used as a correction factor. See items below.

2. Determined that it can operate at 600 ohms even though mismatched.

c. Make connections to the appropriate GND, IN, and OUT binding posts at the top of the set.

d. Place WTG switch on EXT position.

e. Proceed as before. See paragraphs 4.01 through 4.08.

f. If insertion loss is greater than 2 db, the excess loss

can be compensated for by setting the REF LEVEL for all three channels to numbers lower than normal by this amount.

g. Example: It is desired to count impulses at levels of 40, 46, and 52 dbrn. A filter is to be used that has 6 db insertion loss. Since 6 db is 4 db higher than the 2 db for which the set is calibrated, this is 4 db excess loss. To compensate for this we set the REF LEVEL for each channel to be 4 db more sensitive. Thus, the settings sould be 36 (30 + 6), 42 (30 + 12), and 48 (30 + 18) for the three channels.

4.16 To Measure Noise to Ground

a. Make all connections and settings as necessary according to previous paragraphs.

b. Connect a strap between the terminal marked GND and an office ground. This should be to the frame or other good ground.

c. Set INPUT to N-GND position.

d. All other operations and readings are made normally.

5.0 MAINTENANCE

5.01 a. The schematics and photographs identify and locate boards, circuits, and major components. Waveforms and voltages appear on the schematics. Components are identified by lettered symbols according to the following convention:

B	Battery points
C	Capacitor
CR	Diode
E	Printed circuit board
J	Jack or connector
L	Inductor
Q	Transistor
R	Resistor
RY	Solenoid - coil in counter
S	Switch
T	Transformer
TH	Thermistor
W	Waveform

b. Other letters appear which identify points on the printed circuit boards or other panels. These are not associated with components and do not carry numbered suffixes.

c. The set can be removed from the case by loosening the four screws indicated by the arrows. POWER should be OFF.

d. Lift the set straight out of the case, using reasonable care.

CAUTION: If the set is or has been operating on 48 volts for any length of time, resistors R42 and R42A (see Figure 11) may become rather warm. To avoid possible discomfort, avoid contact with these resistors.

5.02 In the event of a malfunction it should be insured that:

a. The set has sufficient power.

b. That all plugs are properly wired and that they are in the proper jacks.

c. All switches are in the proper positions.

d. The set is properly calibrated - see Paragragh 4.13.

5.03 DC Voltage Checks

a. Quite often the obvious faults can be determined by measurements of the DC voltages indicated on the schematics.

b. These voltages are predominantly associated with the transistor stages and a sufficient number are supplied to check all stages.

c. These are measured with no signal input and a 20,000 ohms per volt meter (on approximately 10 or 20 volt scales). They may vary ±25% in normal operation. Gross differences from those indicated warrant further investigation of the individual stage and associated components.

d. While the DC voltage points are not specifically identified on the photographs, the Q numbers of all transistors are, along with either the R or C numbers (or both) of the components where the voltage is to be measured.

e. The schematics also show on which board the stage is located. Initially it may be helpful to first find the board in this manner from Figure 9.

Example: To Measure the collector voltage of Q6:

1. Figure 4, the schematic, shows this should be 7 volts and can be measured at one end of either R34, C26, R35, the collector of Q6, or the base of Q7.

2. Figure 4 also indicates that this stage is located on PC Board E95045.

3. Figure 9 shows the physical location of this board.

4. Figure 11 locates the major components on this board. Q6 and Q7 can be found. The associated components can be found by their physical proximity and observing the foil connections.

5.04 NOTE: Unless otherwise specified, the following paragraphs are with the set in the following operation.

a. A 1 KC sine wave input to the LINE connection at a level of -19 dbm.

b. INPUT on 600 ohms.

c. BRDG/TERM on TERM.

d. HOLD ON/OFF on OFF.

e. WTG on FLT.

f. REF LEVEL on 70.

Channel A on 4

Channel B on 20
Channel C on 20

g. With TIME in CW position, Counter A should be counting or on the verge of counting. Changing its attenuator from 4 to 2 should definitely make it begin counting.

NOTE: There is a built-in delay of approximately 20-30 seconds after the power is turned on by the TIME switch before counting can begin. This is normal and not a malfunction.

5.05 Check Each Channel

a. Each channel can be checked:

1. If Channel A counts as indicated in paragraph 5.02, put Channel A on 2 db.

2. Set Channel B on 2 db and it should begin counting (it may begin on 4 db).

3. Leaving Channels A and B on 2 db, set Channel C on 2 db. This should now count.

b. If no channel operates, the fault is either loss of gain (see paragraph 5.06), Channel A inoperative (see paragraph 5.07), or a timing circuit malfunction (paragraph 5.07).

c. If Channel A operates but B or C do not, then gain is probably correct and the problem is in a channel (either B or B and C). The correct operation of Channel A indicates that both the TIMING and RESET monos are properly operating.

d. If Channels A and B operate while C does not, then the problem involves Channel C only.

5.06 Loss of Gain (See Block Diagram Figure 2)

(A loss sufficient so that CAL controls do not have enough range.)

a. A measurement of the GAIN of the set can be made by putting a high impedance bridging type meter (input impedance greater than 10 K) at the output of Amp 2 (see Figures 4 and 11).

b. Under the conditions of paragraph 5.04 this level should produce a reading of -20 db (±2 db) on the meter when it is set to bridge a 600 ohm circuit.

NOTE: This is not strictly a power reading but a relative db reading. It can also be made in volts where the reading as indicated would be approximately .077 volts RMS.

c. Should the reading of 5.06 b be significantly lower than indicated, the level can be traced backward toward the input as outlined in the following steps.

d. Step 5.06 b reads low, measure the input of Amplifier 2 (see Figures 4 and 11). This should be -55 db ±2 db.

e. Should step 5.06 b be low and step 5.06 d be normal, then Amplifier 2 is not providing sufficient gain (see paragraph 5.09).

f. If step 5.06 d is also low, the trouble is ahead of Amplifier 2. Check the output of Amplifier 1 to be -33 db (see Figures 4 and 9).

g. Should the output of Amplifier 1 be normal (step f) while the input of Amplifier 2 is low (step d), then the trouble is either in the weighting circuits or the attenuator section ahead of Amplifier 2.

h. The input of Amplifier 1 can be checked if necessary. This level is approximately -69 db.

CAUTION: Great care must be used to measure at this level. Normal precautions must be made insofar as extraneous pick up, coupling from high level stages with resulting oscillations. The input to Amplifier 1 is also high impedance (approximately 25 K). Unless a high input impedance meter is now used (half meg), significant loading errors may be introduced.

5.07 Inoperative Channel

a. A CRO is now necessary. This should have an input impedance of at least 1 meg, a capacitance, including leads, of less than 100 pf, a bandwidth in the order of 100 KC or more, and a vertical sensitivity that will display 250 MV and have a DC input.

b. Reference is made to Figure 5, which shows the schematic of Channel A, and Figure 14, which shows the physical location of some key points and parts. This schematic is usable for trouble shooting all three channels, the major difference being the output connections.

NOTE: Due to the manner of interconnections, counter operation cannot be normal unless Channel A is operating at least through the gate (W5).

c. Switches are to be as indicated in paragraph 5.04 except as indicated in step d below.

d. If Channel A is being tested, then all of paragraph 5.4 is proper. If Channel B is being tested, set B attenuator at 4 db and A attenuator at 4 db, C attenuator is on 20 db. If Channel C is being tested, place all three channel attenuators on 4 db. See note in step b above.

e. Observe the 1 KC input at point J (W1) to be 100 MV p-p.

f. Observe W2 to be approximately 500 MV p-p. Note that this is at 2 KC, due to the phase splitting action.

g. Observe the waveform, W4. The level here is not too critical, but the time is critical to give the proper count rate which is approximately 10 per second.

h. Observe waveform W5 gate output

i. Observe waveform W6 across the counter.

j. Up to and including waveform W2, the circuitry is fairly straightforward and in the event of missing or reduced signals the cause can be determined in normal trouble shooting techniques.

k. If W2 is present and at proper level but subssequent waveforms are missing, then the malfunction is in the pulse circuitry.

5.08 Pulse Circuit Malfunction

a. For missing W4.

b. Remove signal, monitor at the point for W4 with a DC CRO and turn POWER off for 15 seconds.

c. Turn power on and wait 30 seconds. Voltage at this point must be low--near ground. If this voltage is negative (near 6 volts), Q104 may be open.

d. Increase signal level to normal (or a few db higher).

e. If the point for W4 (the collector of Q104) stays near ground or follows the signal, the problem is in this SET/RESET multivibrator.

f. If the point for W4 flips to a negative voltage (about 6) and stays there, then the SET/RESET mono is not being reset.

5.09 Timing Mono Check (Figures 7 and 14)

a. When the SET/RESET of LO LEVEL (A) Channel flips on signal, but is not reset.

b. Place DC CRO on the point for W9 (Q402 collector).

c. Turn power OFF for 15 seconds and then reapply.

d. Observe carefully as power is applied, after some 20 or 30 seconds, a single pulse of some 40 msecs should occur. The time duration of this need not be observed, only that the pulse exists. It is best observed on a CRO with either no sweep or a fast sweep so that the pulse does not occur during retrace.

e. Apply signal and observe if another single pulse occurs.

f. If the pulse occurs for either steps d or e, the problem is not in the TIMING mono (see RESET below). If the pulse occurs for step d but not step e, the SET/RESET is not triggering the TIMING mono.

5.10 RESET Mono Check

a. The TIMING mono checks OK but the SET/RESET is not being reset.

b. Place the DC CRO so as to observe W11 (Figures 7 and 14).

c. Turn power off for 15 seconds. Reapply power, with no signal input, and carefully observe a single positive going pulse after 20 or 30 seconds.

d. Apply signal and observe another single pulse.

e. If the TIMING was operating and c and d do not produce pulses, the RESET mono is not functioning properly.

5.11 Gate Check

a. Malfunction of a gate or gates will normally show up with the wrong counters operating or no counters operating.

b. The gate diodes can be checked with an ohmmeter.

CAUTION: Certain brands of ohmmeters produce high voltages and/or currents which may damage the circuit. An ohmmeter which delivers no more than 1.5 volts or 10 ma is advisable. A typical meter is the Triplett 630 series on the X 1 K range.

c. Measure the resistance of each diode (total of 12) in gates with both polarities. This can be done without removing the diodes.

CAUTION: Be sure the power is off.

d. Normal readings will be approximately 800 ohms and 14 K for the two polarities.

e. A shorted diode will produce lower readings in both polarities.

f. An open diode will produce readings of approximately 4 K and 14 K for the two polarities.

5.12 Power Station Check

a. Check B1 to be 18 volts (±2 volts).

b. Check B2 to be 12 volts (+1, -2 volts).

c. With 18 volts read at B1 if B2 is 18 volts, check the base of Q405.

1. If Q405 base is 12 volts, the transistor is probably open.

2. If Q405 base is 18 volts, CR405 may be open.

CAUTION: When replacing transistors, always turn off the power for at least 15 seconds before inserting the transistor in its socket. This allows discharging of all capacitors and prevents excessive peak voltages and/or currents from being applied to the transistors.

d. If B2 is less than 12 volts:

1. B2 may be drawing excessive current; to check this disconnect from each board by unsoldering the wire connected to B2 (do not let these unsoldered ends touch anything).

2. CR405 or C407 may be defective.

e. Check B3 to be 9 volts (+1, -2 volts).

f. Apply checks similar to sub-paragraphs c and d to B3, Q406, CR406, and C408.

g. 48 volt check

1. Apply 48 volts DC to the prescribed jack.

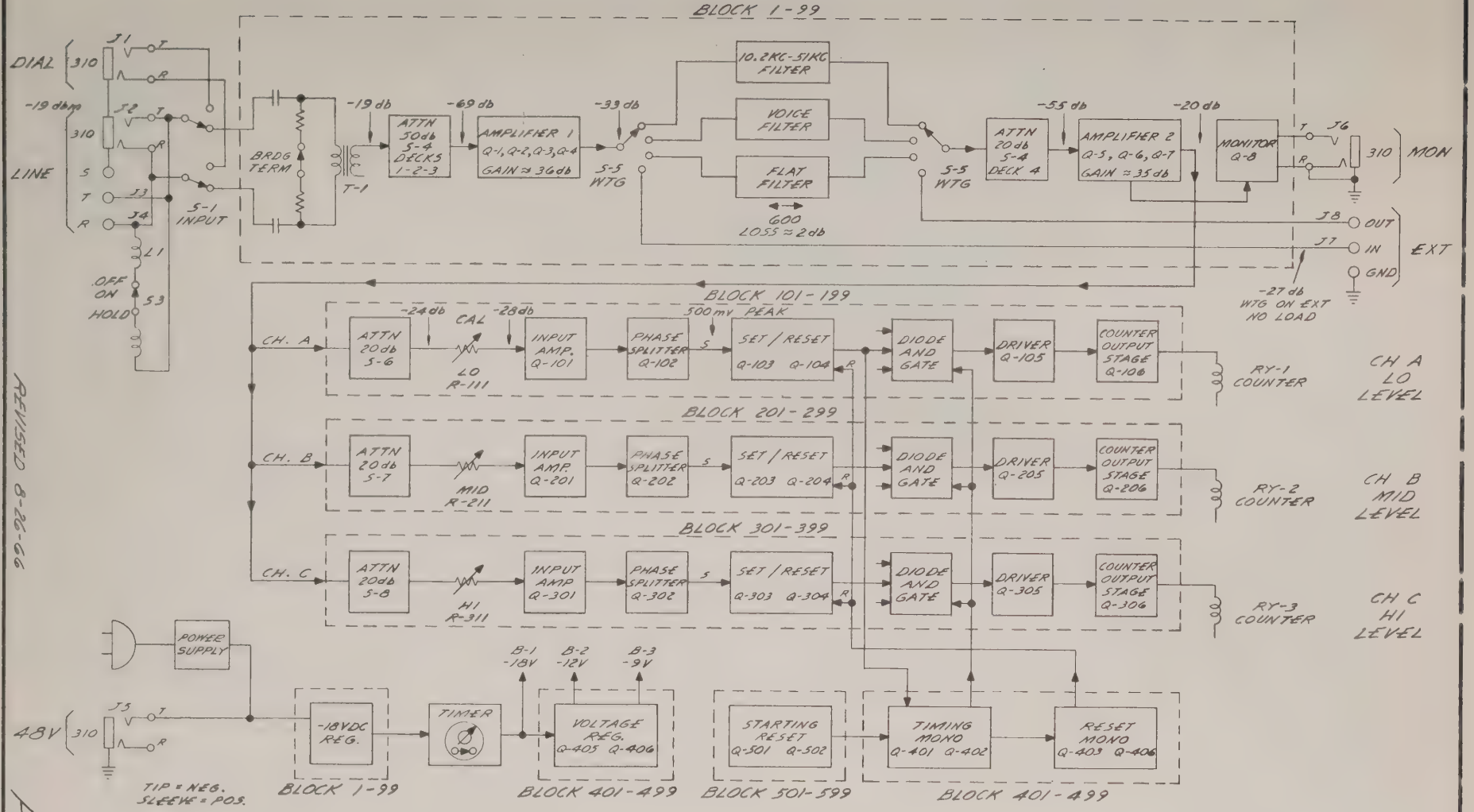
   CAUTION: Always connect to the TTS 58ARP first, then the 48 volts. Reversal of this procedure may result in a blown fuse in the 48 volt supply.

2. Measure the voltage across CR2 to be 18 volts (±2 volts).

3. Place power on by turning the TIME switch clockwise, POWER switch ON.

4. Determine that B1 has 18 volts present.

5. If the voltage at B1 is missing, check presence of voltage and polarity at anode end of CR1 (Figures 3 and 11).

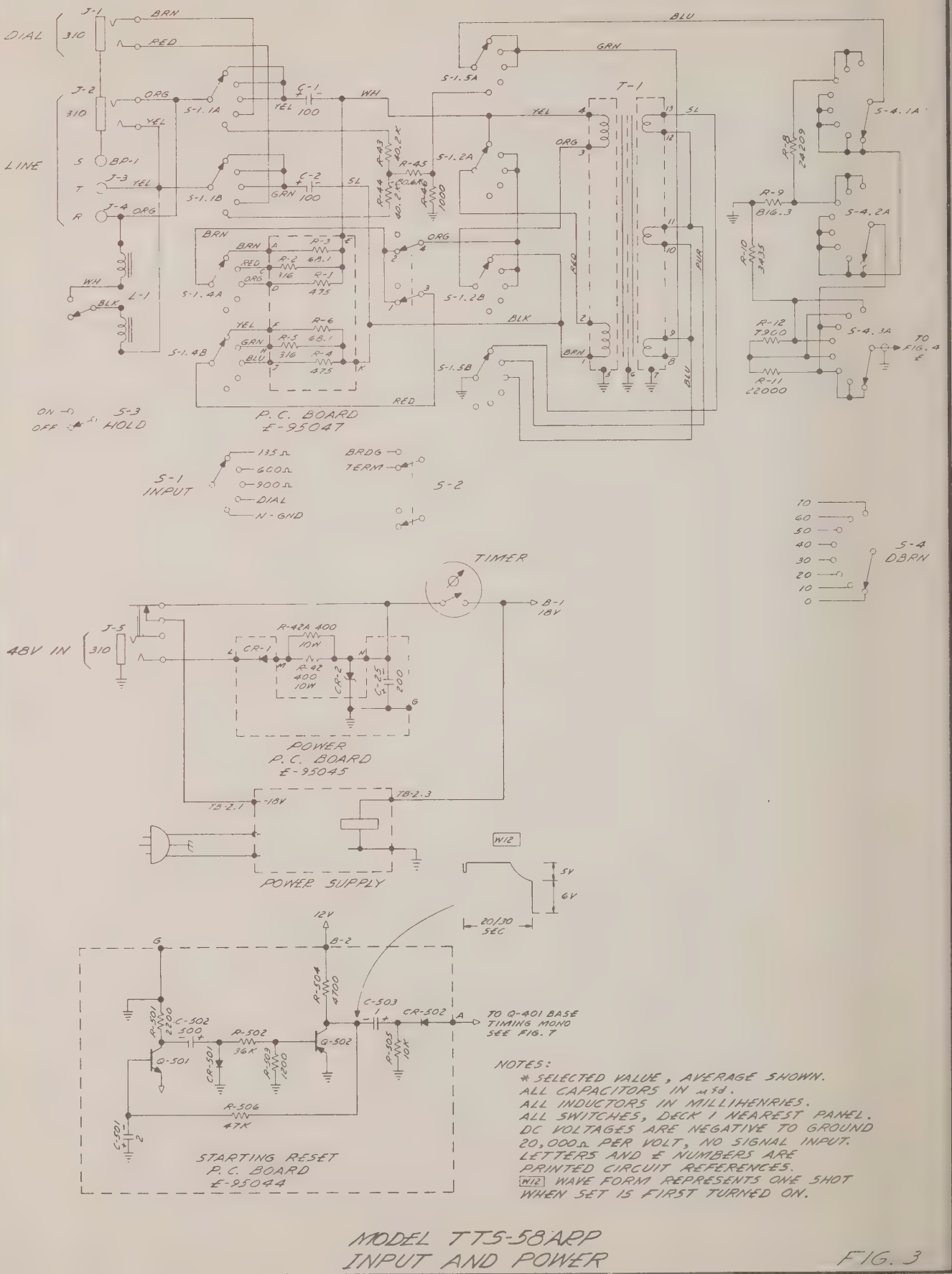


REVISED 8-26-66

FIG. 2

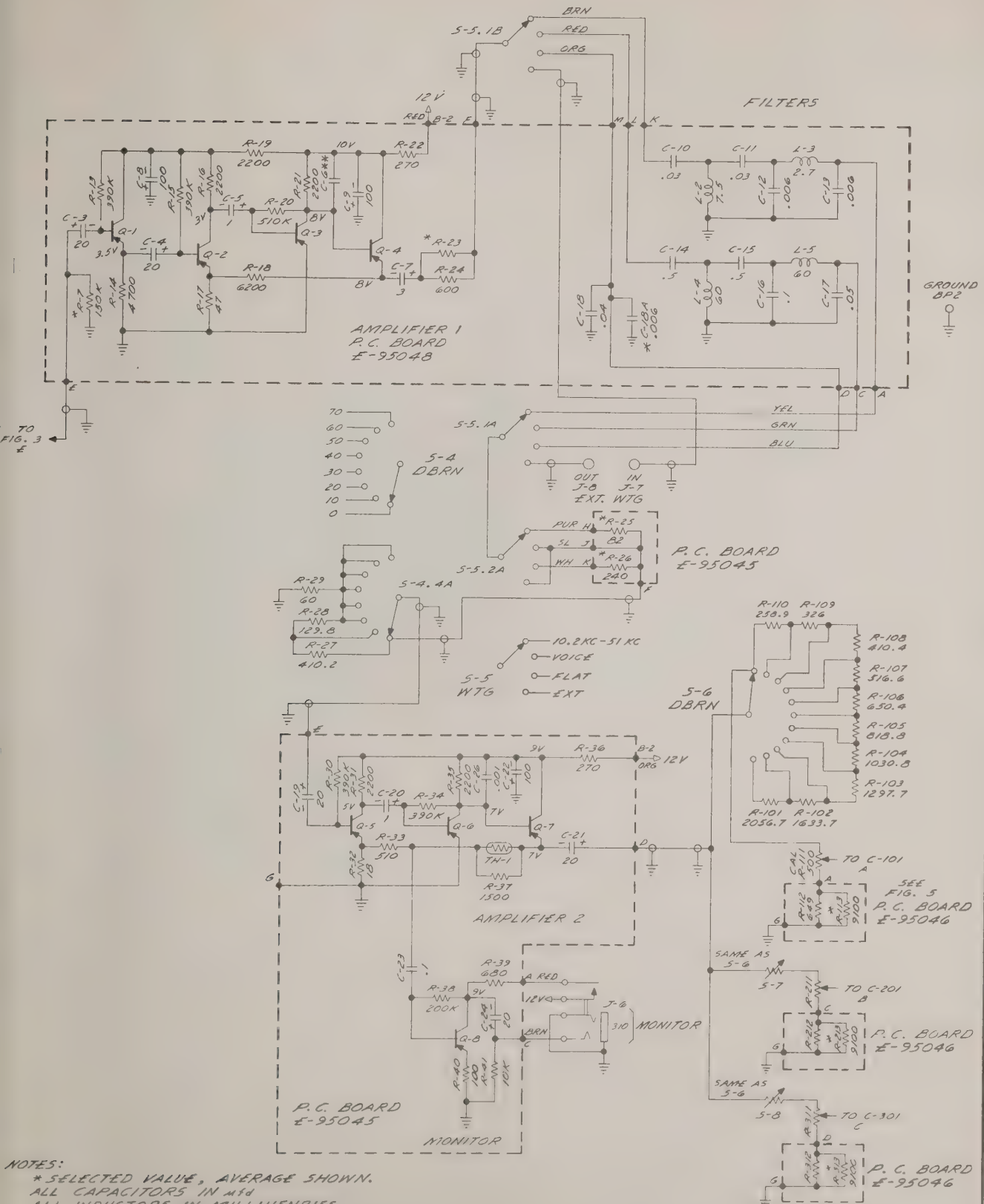
MODEL TTS-58ARP
BLOCK DIAGRAM

LEVELS INDICATED ARE FOR 1KC, -19 dbm INPUT LEVEL. WITH ATTENUATORS SET FOR 74 dbrn. FLAT FILTER POSITION. MAIN ATTEN. SET TO 70 dbrn. CHANNEL A SET TO 4 dbrn



MODEL TTS-58ARP
INPUT AND POWER

FIG. 3



NOTES:
* SELECTED VALUE, AVERAGE SHOWN.
ALL CAPACITORS IN mfd
ALL INDUCTORS IN MILLIHENRIES
ALL SWITCHES, DECK 1 NEAREST PANEL.
DC VOLTAGES ARE NEGATIVE TO GROUND
20,000Ω PER VOLT, NO SIGNAL INPUT
LETTERS AND # NUMBERS ARE
PRINTED CIRCUIT REFERENCES.
** SELECTED VALUE, MAY BE OMITTED.

MODEL TT5-58ARP
AMPLIFIERS AND MONITOR

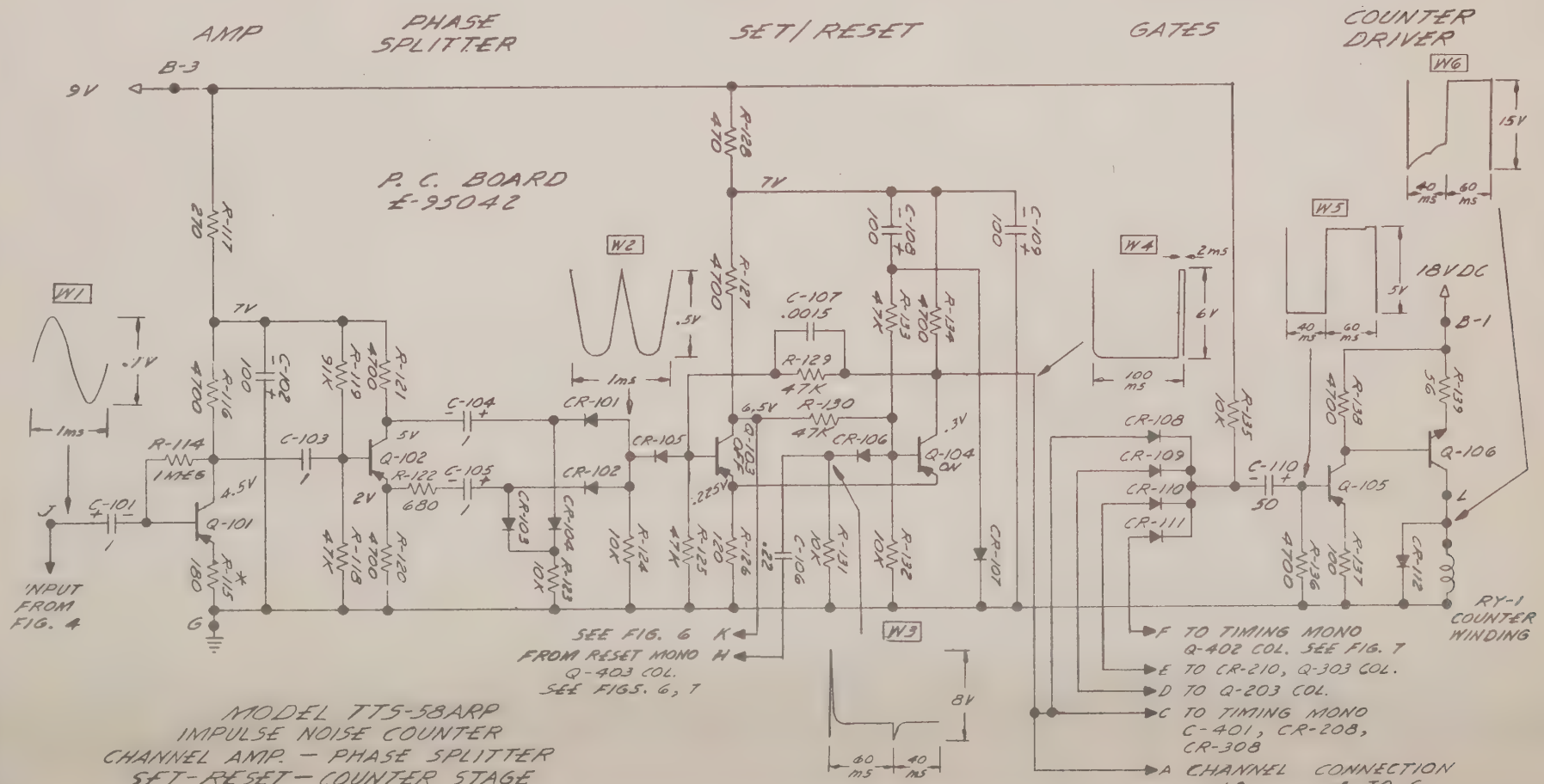
REVISED 8-26-66

FIG. 4

LO CHANNEL = 101 — 199 BLOCK
MID CHANNEL = 201 — 299 BLOCK
HI CHANNEL = 301 — 399 BLOCK

LO CHANNEL SHOWN

NOTES:
ALL CAPACITORS IN Mfd
DC VOLTAGES ARE NEGATIVE TO GROUND
20,000 PER VOLT. NO SIGNAL INPUT.
LETTERS AND E NUMBERS ARE
PRINTED CIRCUIT REFERENCES.
* SELECTED VALUE, AVERAGE VALUE SHOWN.
WAVE FORMS ARE SHOWN FOR A 1000 cps
SINE WAVE INPUT.
ALL THREE CHANNEL PRINTED CIRCUIT BOARDS
NUMBERED 101-199 BLOCK. 200 AND 300 BLOCK
NUMBERS ARE SCHEMATIC REFERENCES ONLY.

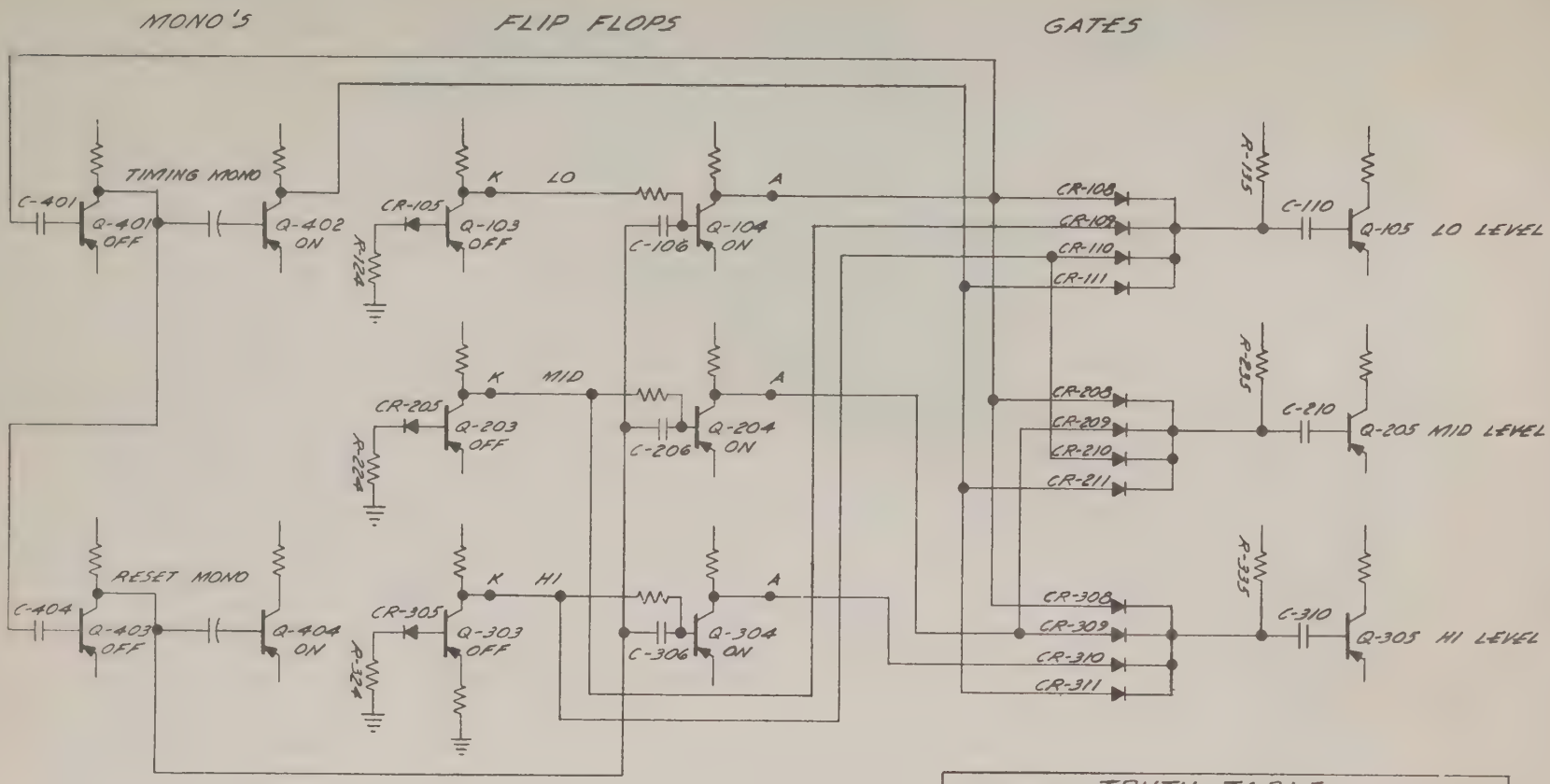


MODEL TTS-58ARP
IMPULSE NOISE COUNTER
CHANNEL AMP. — PHASE SPLITTER
SET-RESET — COUNTER STAGE
3 CHANNELS

REVISED 8-26-66

FIG. 5

NOTES:
ON/OFF STATES INDICATES NO SIGNAL CONDITIONS.
ALL THREE CHANNEL PRINTED CIRCUIT BOARDS NUMBERED 101-199 BLOCK. 200 AND 300 BLOCK NUMBERS ARE SCHEMATIC REFERENCES ONLY.

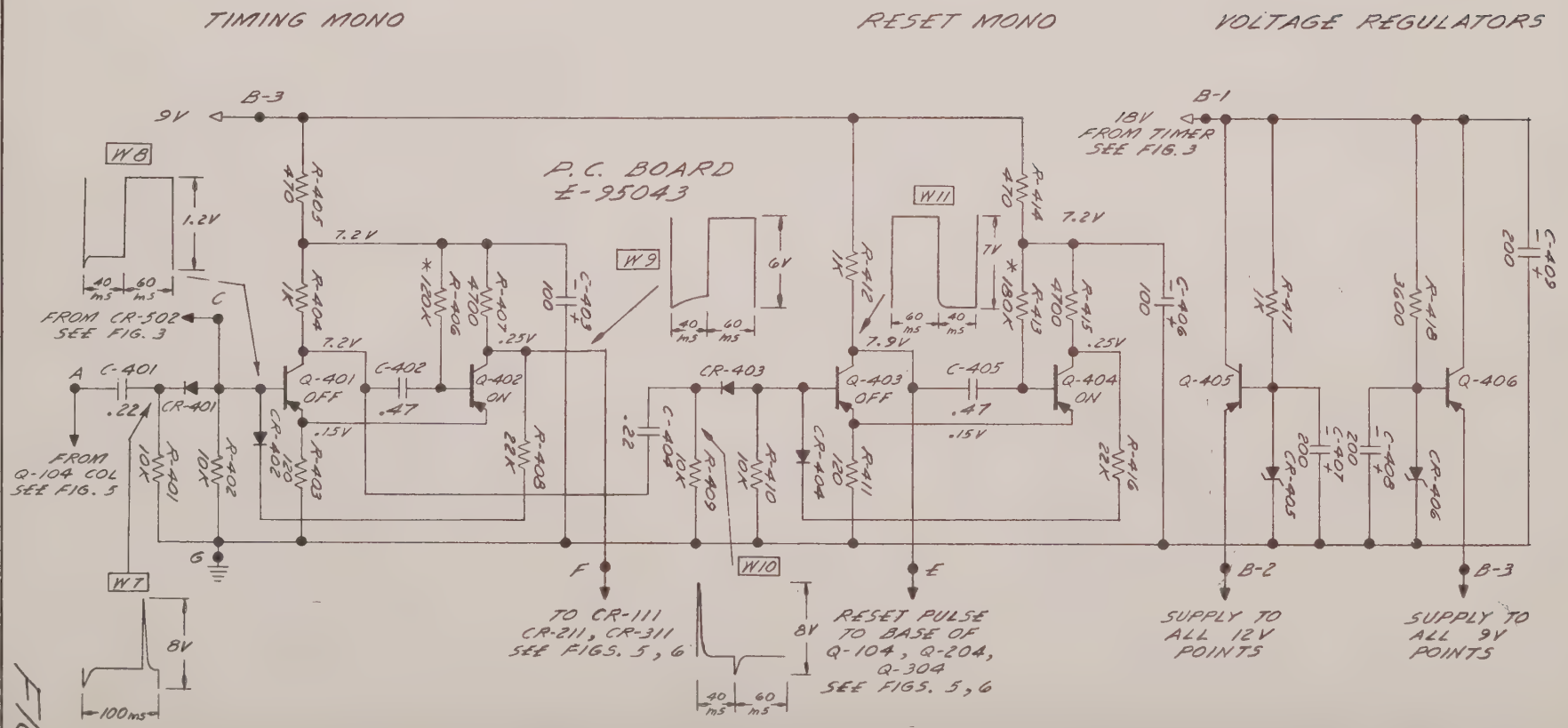


TRUTH TABLE	
GATE OUTPUT	WITH THESE STAGES ON
LO	Q-103-204-304-401
MID	Q-103-203-304-401
HI	Q-103-203-303-401

MODEL TT5-58ARP
INTERCONNECTIONS

FIG. 6

NOTES:
ALL CAPACITORS IN μfd
DC VOLTAGES ARE NEGATIVE TO GROUND
20,000Ω PER VOLT. NO SIGNAL INPUT.
LETTERS AND E NUMBERS ARE
PRINTED CIRCUIT REFERENCES.
* SELECTED VALUE. AVERAGE VALUE SHOWN.
WAVE FORMS ARE SHOWN FOR A 1000 cps
SINE WAVE INPUT.



MODEL TTS-58ARP
IMPULSE NOISE COUNTER
TIMING MONO - RESET MONO
REGULATOR STAGES

FIG. 7

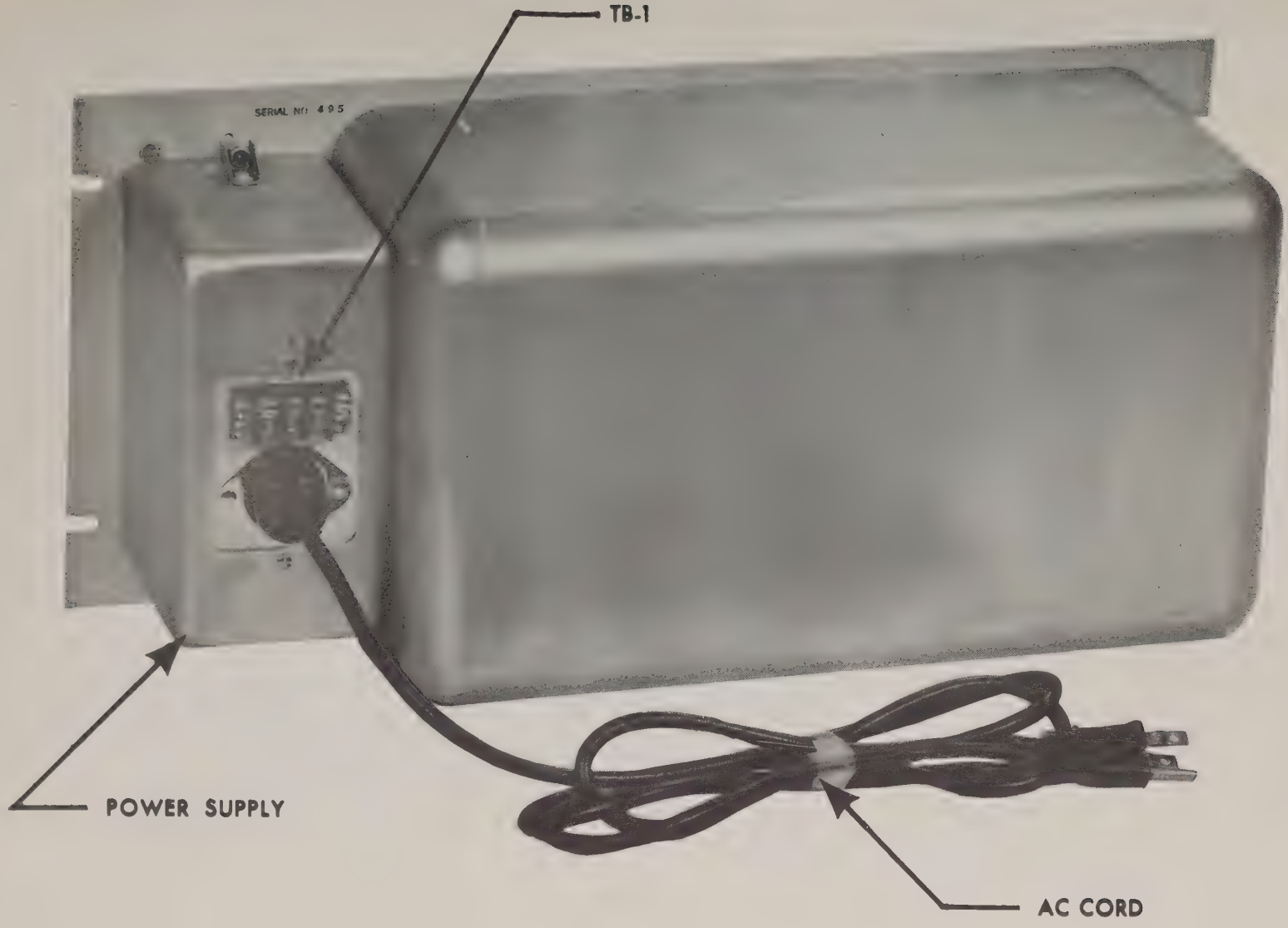


FIG-8

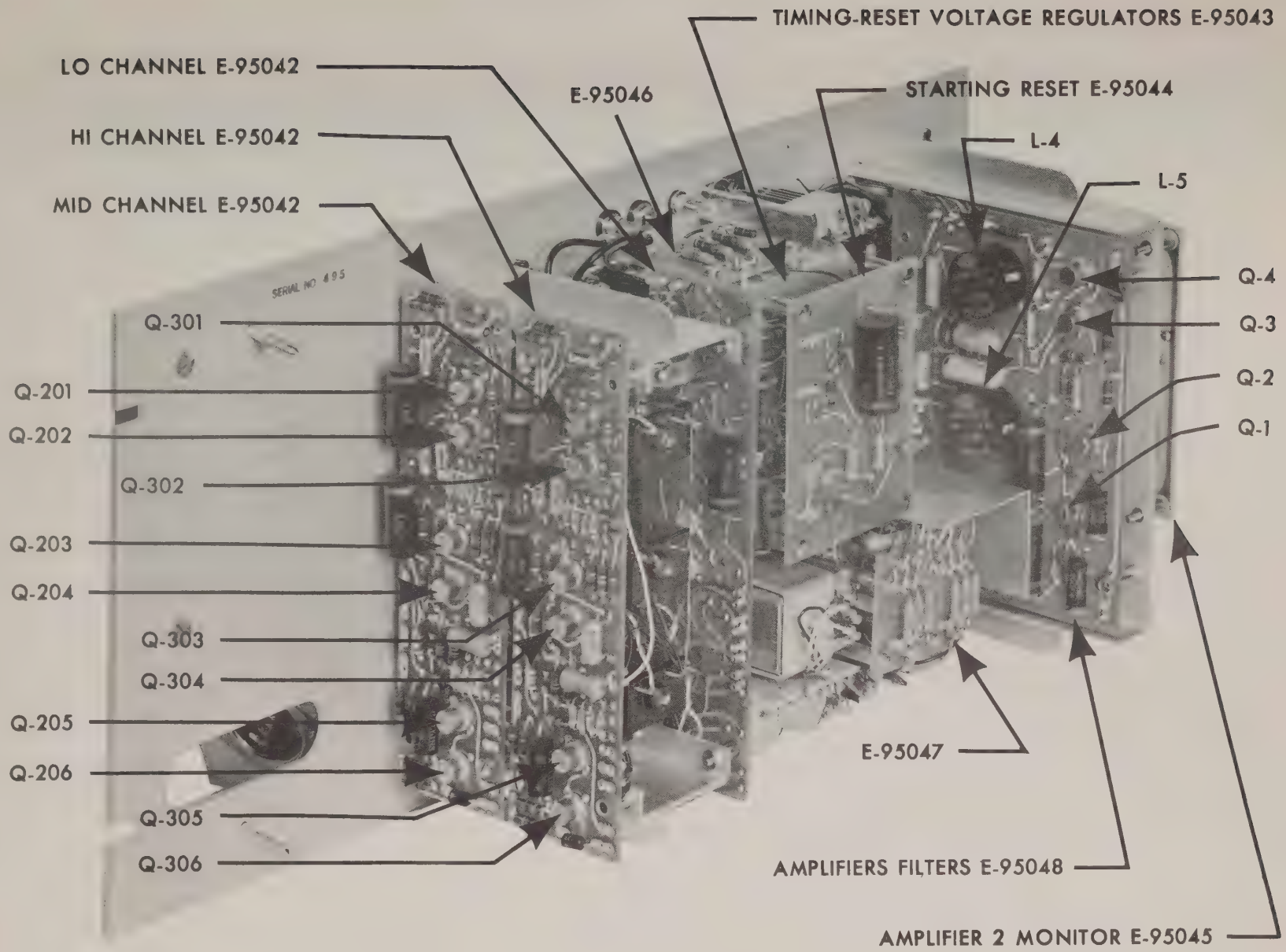

TIMING-RESET VOLTAGE REGULATORS E-95043
LO CHANNEL E-95042
E-95046
STARTING RESET E-95044
HI CHANNEL E-95042
L-4
L-5
MID CHANNEL E-95042
Q-4
Q-3
Q-2
Q-1
Q-301
Q-201
Q-202
Q-302
Q-203
Q-204
Q-303
Q-304
Q-205
Q-206
Q-305
Q-306
E-95047
AMPLIFIERS FILTERS E-95048
AMPLIFIER 2 MONITOR E-95045

FIG-9

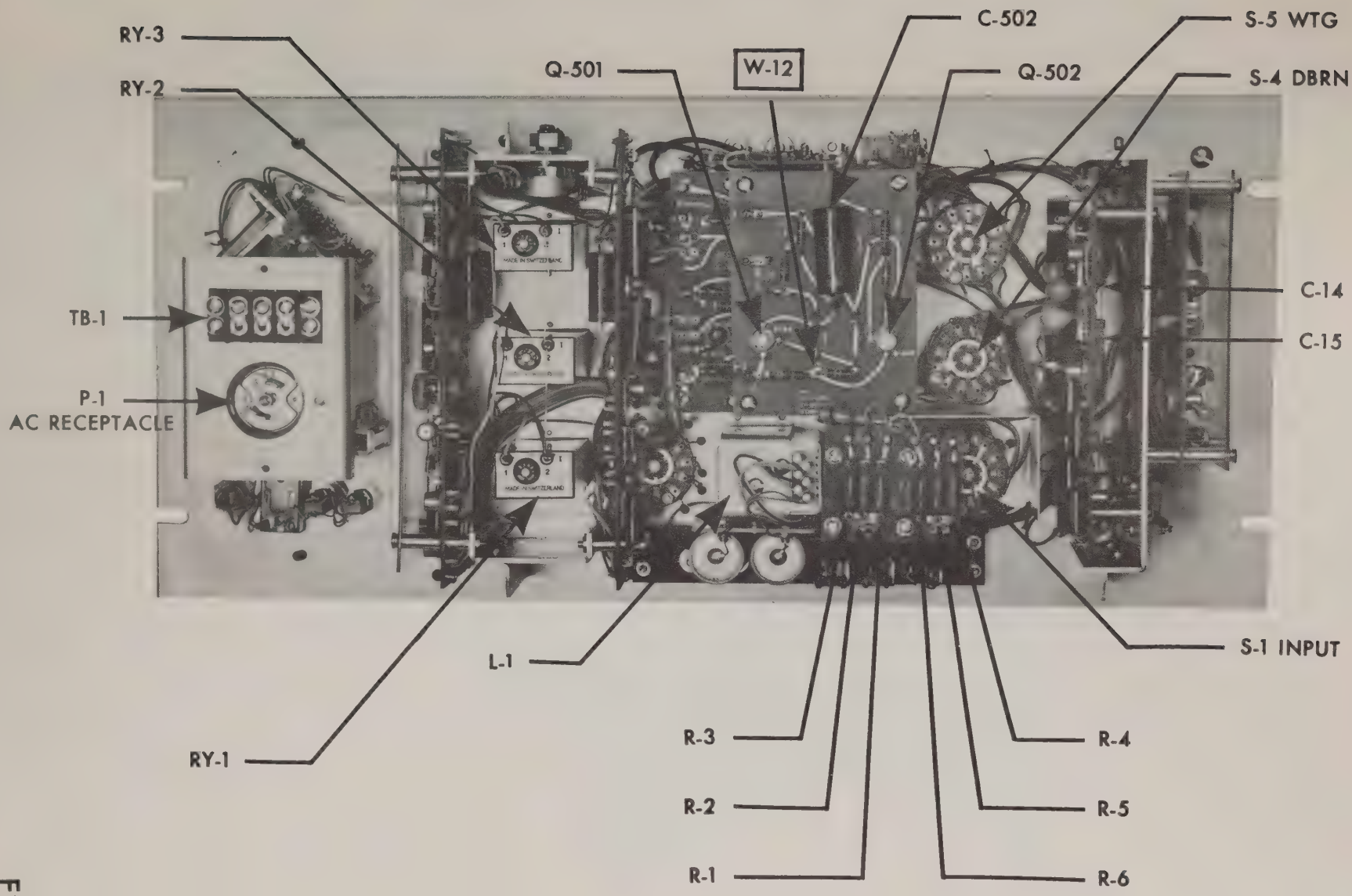

RY-3
RY-2
Q-501
W-12
C-502
Q-502
S-5 WTG
S-4 DBRN
C-14
C-15
TB-1
P-1
AC RECEPTACLE
L-1
S-1 INPUT
RY-1
R-3
R-2
R-1
R-4
R-5
R-6

FIG-10

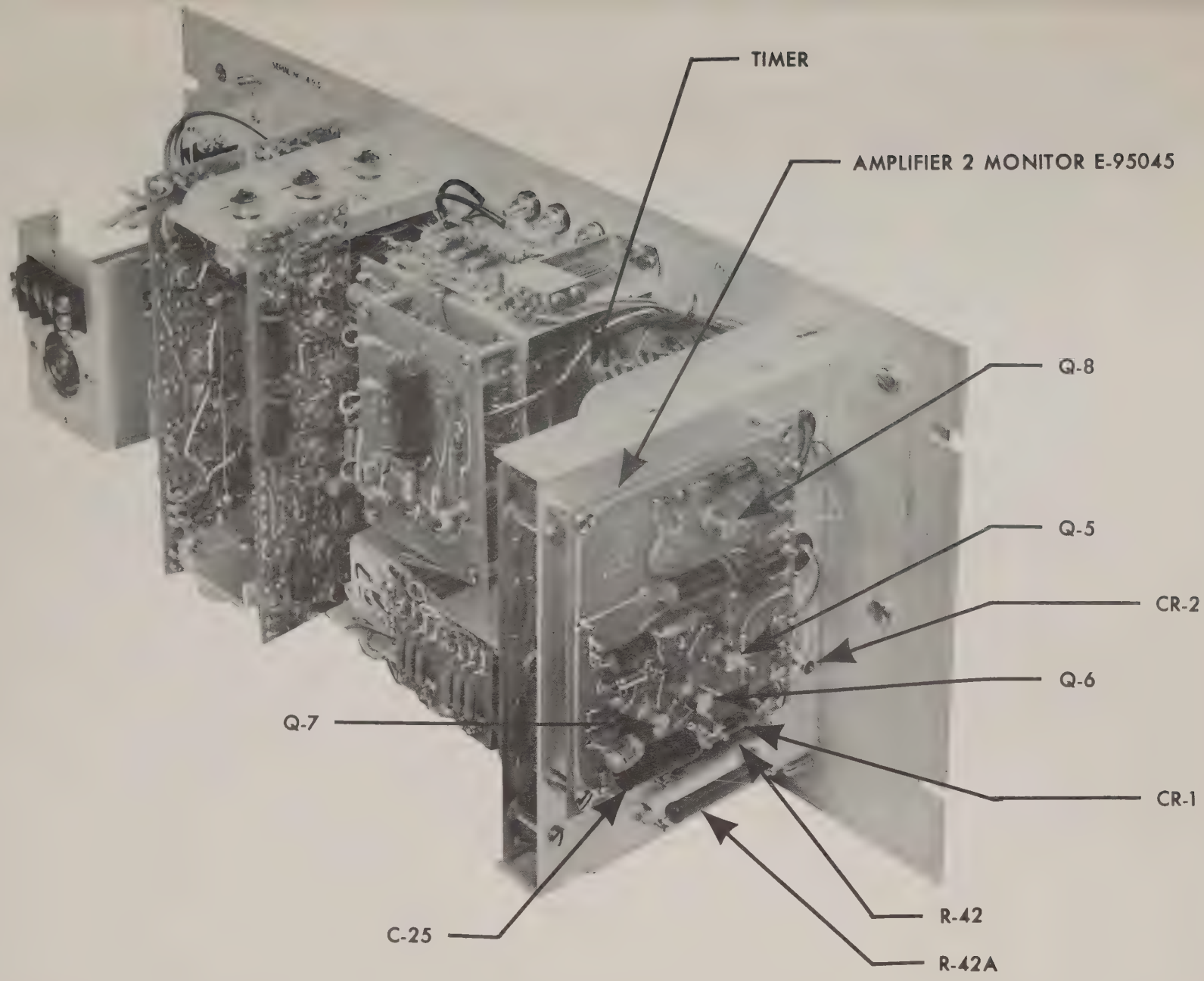

TIMER
AMPLIFIER 2 MONITOR E-95045
Q-8
Q-5
CR-2
Q-6
Q-7
CR-1
R-42
C-25
R-42A

FIG-11

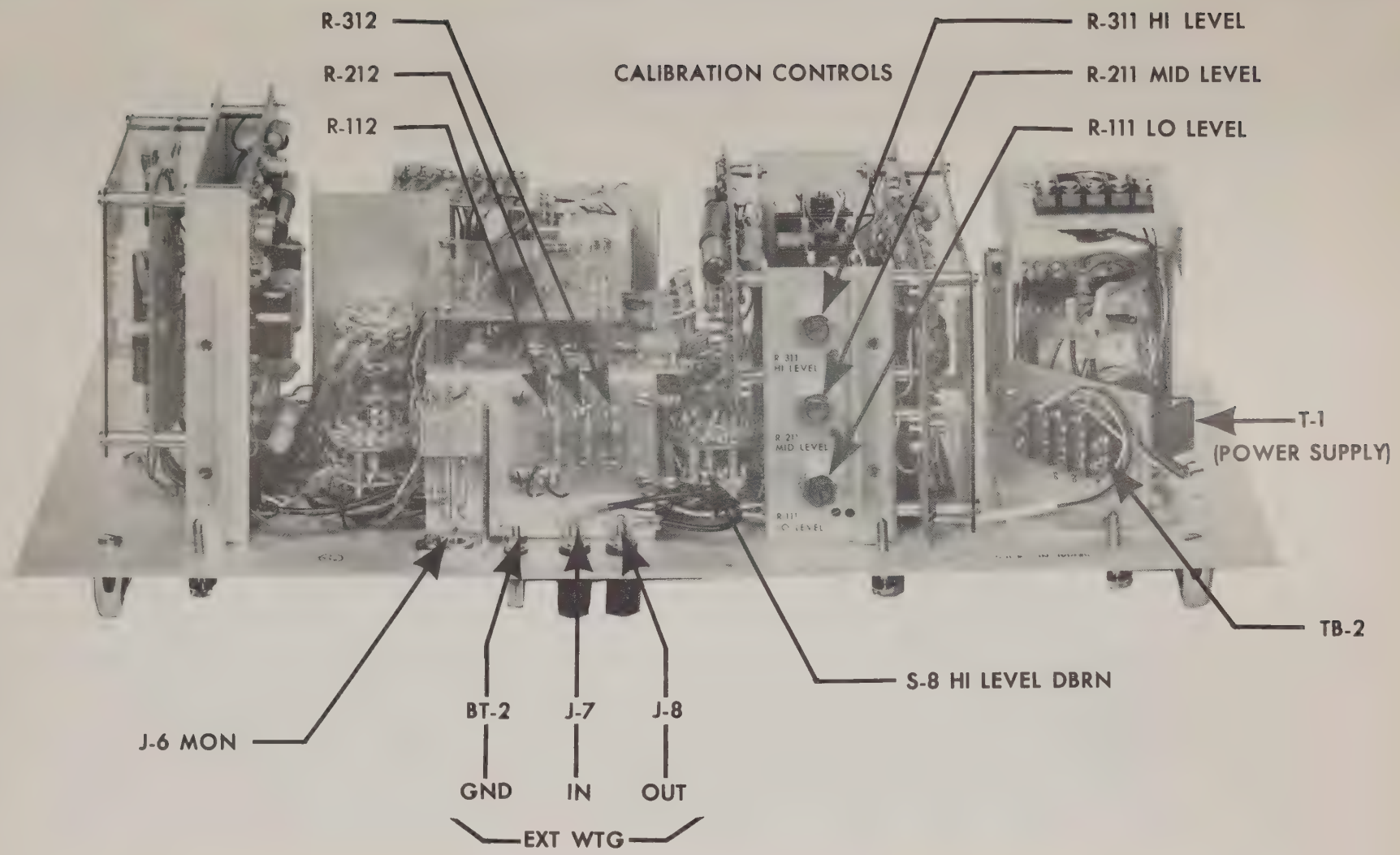

R-312
R-212
R-112
CALIBRATION CONTROLS
R-311 HI LEVEL
R-211 MID LEVEL
R-111 LO LEVEL
T-1
(POWER SUPPLY)
TB-2
S-8 HI LEVEL DBRN
J-6 MON
BT-2
J-7
J-8
GND
IN
OUT
EXT WTG

FIG-12

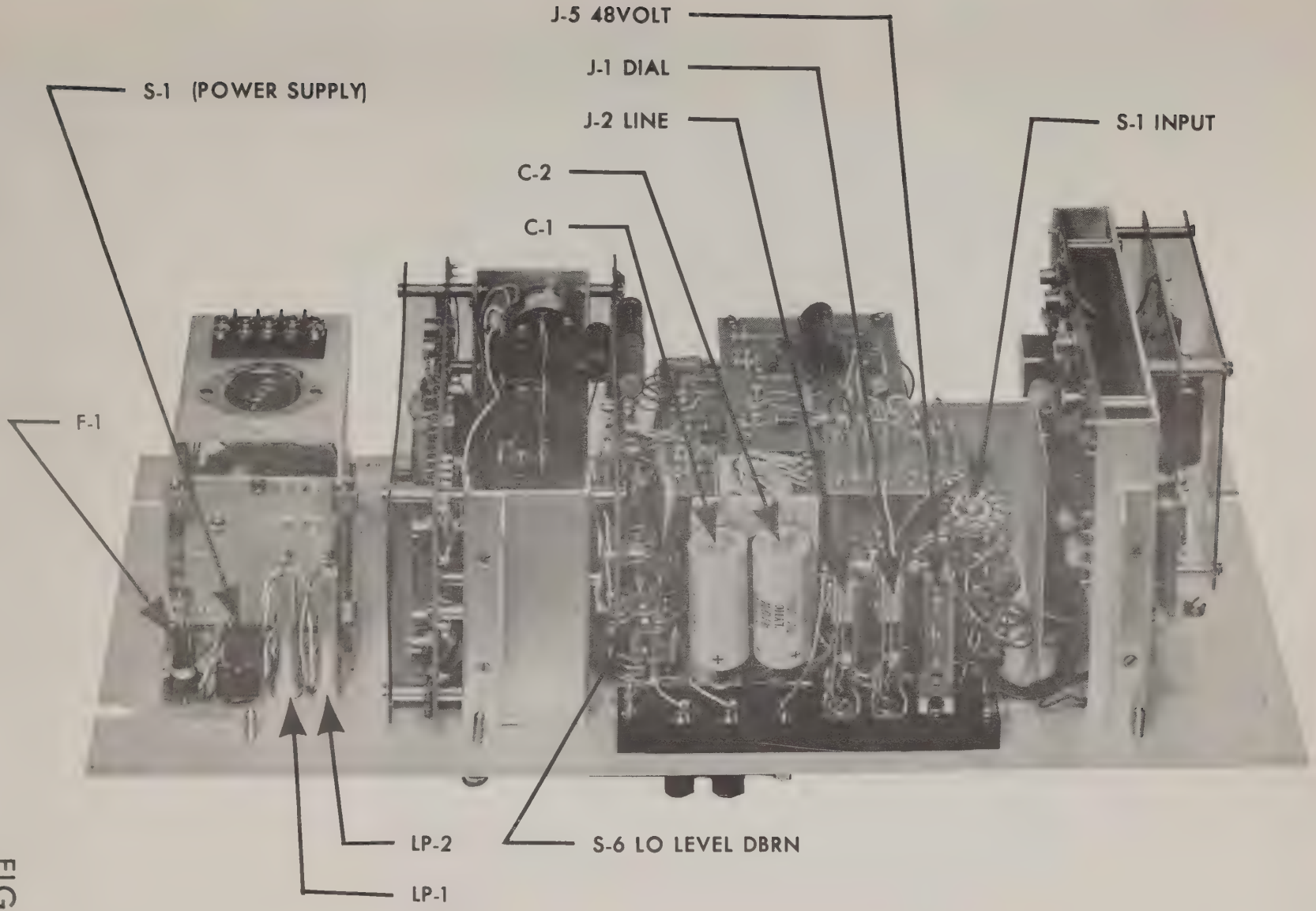

J-5 48VOLT
J-1 DIAL
J-2 LINE
C-2
C-1
S-1 (POWER SUPPLY)
S-1 INPUT
F-1
LP-2
LP-1
S-6 LO LEVEL DBRN

FIG-13

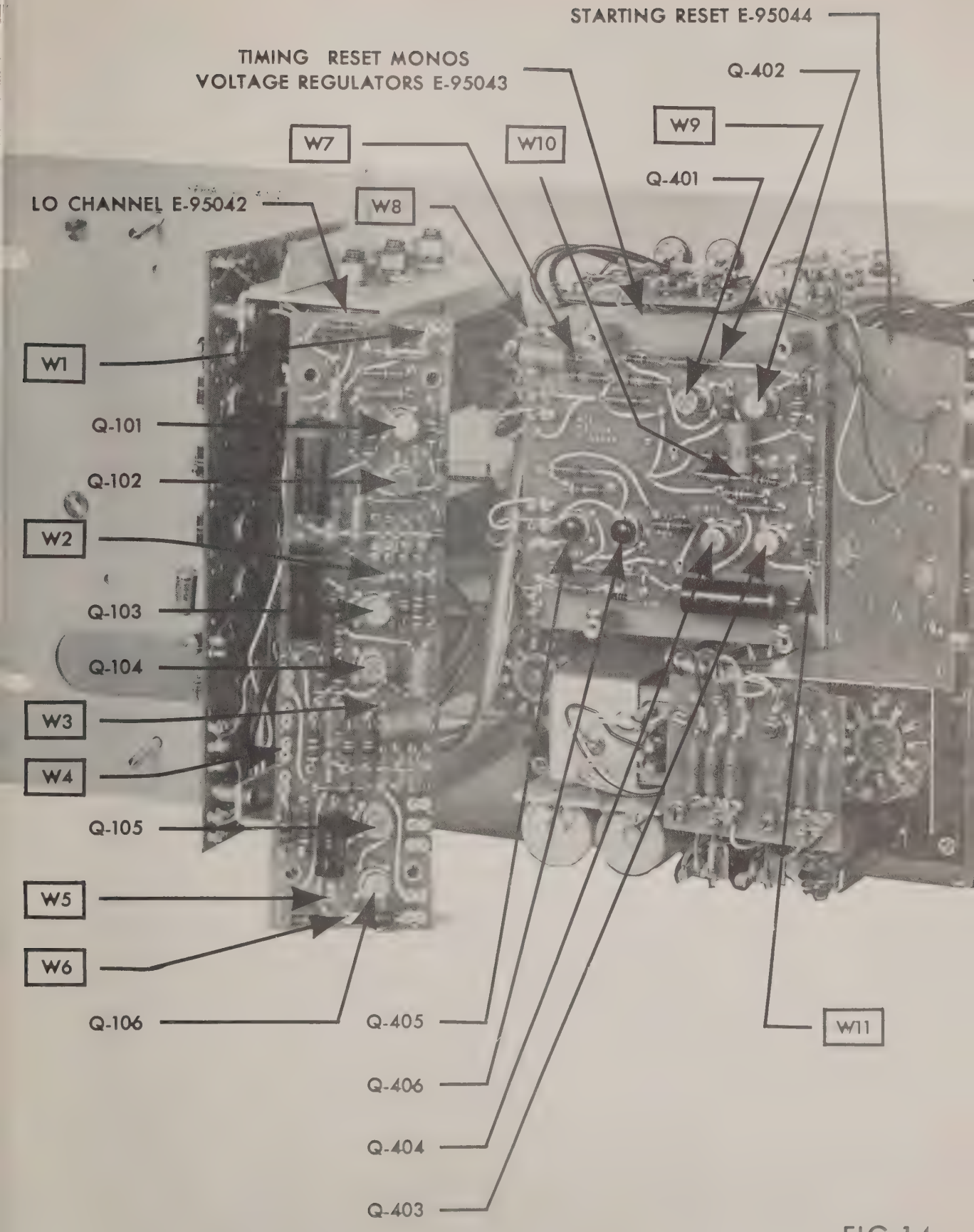

STARTING RESET E-95044
TIMING RESET MONOS
VOLTAGE REGULATORS E-95043
Q-402
W9
W7
W10
Q-401
LO CHANNEL E-95042
W8
W1
Q-101
Q-102
W2
Q-103
Q-104
W3
W4
Q-105
W5
W6
Q-106
Q-405
Q-406
Q-404
Q-403
W11

FIG-14

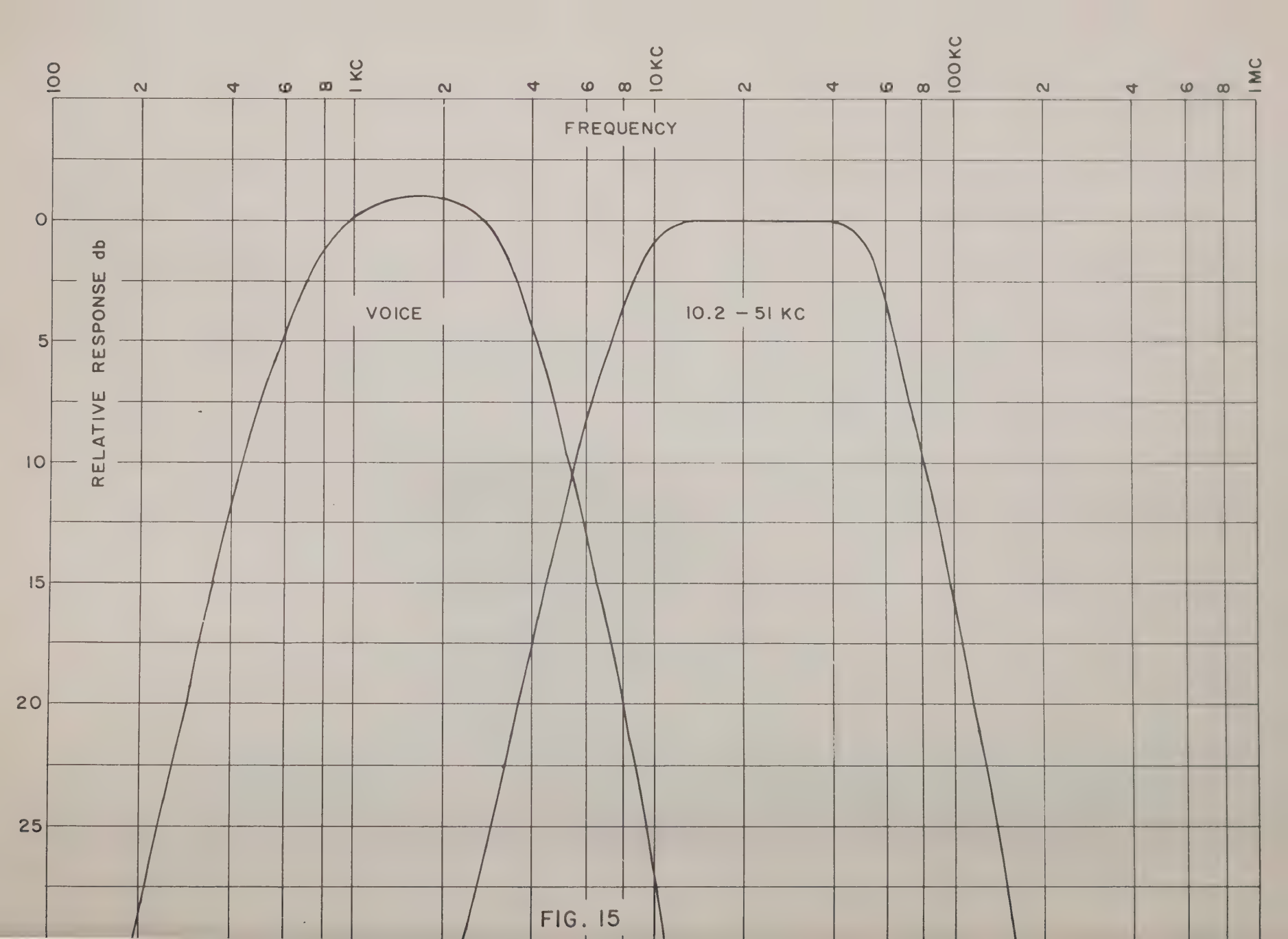

100
2
4
6
8
1 KC
2
4
6
8
10 KC
2
4
6
8
100 KC
2
4
6
8
1 MC
FREQUENCY
RELATIVE RESPONSE db
0
5
10
15
20
25
VOICE
10.2 – 51 KC

FIG. 15

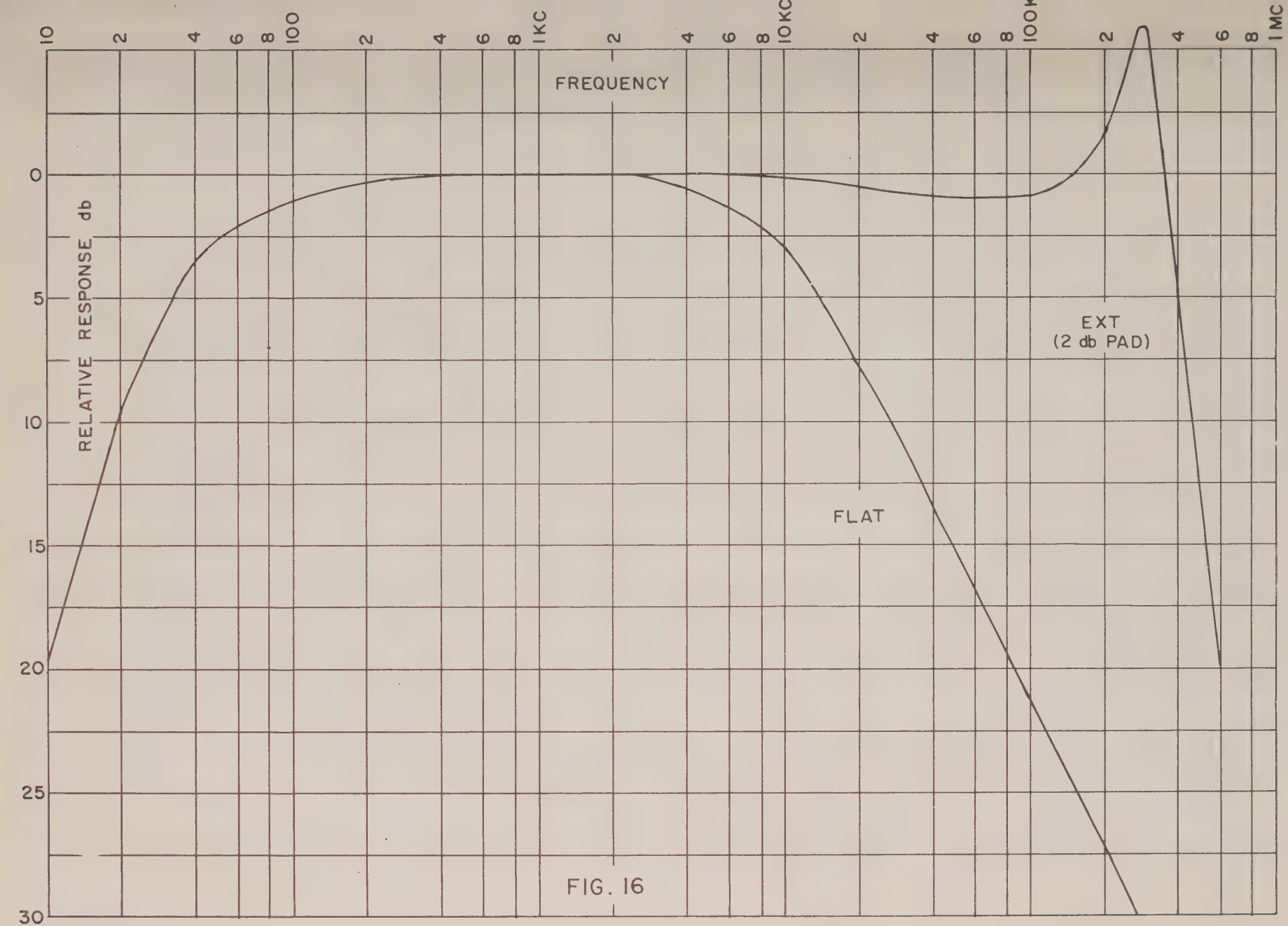

10
2
4
6
8
100
2
4
6
8
1KC
2
4
6
8
10KC
2
4
6
8
100KC
2
4
6
8
1MC
FREQUENCY
0
5
10
15
20
25
30
RELATIVE RESPONSE db
EXT
(2 db PAD)
FLAT

FIG. 16

TABLE OF REPLACEABLE PARTS

Circuit Ref	Description	Mfr* & Mfr's Designation
C1	Capacitor: fixed, electrolytic, 100 mfd, 150 vdc	Y, TVA-1420
C2	Capacitor: fixed, electrolytic, 100 mfd, 150 vdc	Y, TVA-1420
C3	Capacitor: fixed, electrolytic, 20 mfd, 25 vdc	M, APD-046
C4	Capacitor: fixed, electrolytic, 20 mfd, 25 vdc	M, APD-046
C5	Capacitor: fixed, electrolytic, 1 mfd, 15 vdc	Y, TE-1148
C6	Capacitor: fixed, paper, selected value	
C7	Capacitor: fixed, electrolytic, 3 mfd, 15 vdc	Y, TE-1150
C8	Capacitor: fixed, electrolytic, 100 mfd, 20 vdc	M, APD-095
C9	Capacitor: fixed, electrolytic, 100 mfd, 20 vdc	M, APD-095
C10	Capacitor: fixed, paper, .03 mfd, 400 vdc	Y, 4PS-S30
C11	Capacitor: fixed, paper, .03 mfd, 400 vdc	Y, 4PS-S30
C12	Capacitor: fixed, paper, .006 mfd, 600 vdc	Y, 6PS-D60
C13	Capacitor: fixed, paper, .006 mfd, 600 vdc	Y, 6PS-D60
C14	Capacitor: fixed, paper, .5 mfd, 200 vdc	Y, 2PS-P50
C15	Capacitor: fixed, paper, .5 mfd, 200 vdc	Y, 2PS-P50
C16	Capacitor: fixed, paper, .1 mfd, 200 vdc	Y, 2PS-P10
C17	Capacitor: fixed, paper, .05 mfd, 200 vdc	Y, 2PS-S50
C18	Capacitor: fixed, paper, .04 mfd, 200 vdc	Y, 4PS-S40
C18A	Capacitor: fixed, paper, selected value	
C19	Capacitor: fixed, electrolytic, 20 mfd, 25 vdc	M, APD-046
C20	Capacitor: fixed, electrolytic, 1 mfd, 15 vdc	Y, TE-1148
C21	Capacitor: fixed, electrolytic, 20 mfd, 25 vdc	M, APD-046
C22	Capacitor: fixed, electrolytic, 100 mfd, 20 vdc	M, APD-095
C23	Capacitor: fixed, ceramic, .1 mfd, 75 vdc	M, DDA-104
C24	Capacitor: fixed, electrolytic, 20 mfd, 25 vdc	M, APD-046
C25	Capacitor: fixed, electrolytic, 200 mfd, 20 vdc	M, APD-115
C26	Capacitor: fixed, paper, .001 mfd, 600 vdc	Y, 6PS-D10
C101	Capacitor: fixed, electrolytic, 1 mfd, 15 vdc	Y, TE-1148
C102	Capacitor: fixed, electrolytic, 100 mfd, 20 vdc	M, APD-095
C103	Capacitor: fixed, electrolytic, 1 mfd, 15 vdc	Y, TE-1148
C104	Capacitor: fixed, electrolytic, 1 mfd, 15 vdc	Y, TE-1148
C105	Capacitor: fixed, electrolytic, 1 mfd 15 vdc	Y, TE-1148
C106	Capacitor: fixed, ceramic, .22 mfd, 80 vdc	Y, 192P2240R8
C107	Capacitor: fixed, paper, .0015 mfd, 600 vdc	Y, 6PS-D15
C108	Capacitor: fixed, electrolytic, 100 mfd, 20 vdc	M, APD-095
C109	Capacitor: fixed, electrolytic, 100 mfd, 20 vdc	M, APD-095
C110	Capacitor: fixed, electrolytic, 50 mfd, 15 vdc	M, APD-054
C401	Capacitor: fixed, ceramic, .22 mfd, 80 vdc	Y, 192P2240R8
C402	Capacitor: fixed, paper, .47 mfd, 80 vdc	Y, 192P4749R8
C403	Capacitor: fixed, electrolytic, 100 mfd, 20 vdc	M, APD-095
C404	Capacitor: fixed, ceramic, .22 mfd, 80 vdc	Y, 192P2240R8
C405	Capacitor: fixed, paper, .47 mfd, 80 vdc	Y, 192P4749R8
C406	Capacitor: fixed, electrolytic, 100 mfd, 20 vdc	M, APD-095
C407	Capacitor: fixed, electrolytic, 200 mfd, 20 vdc	M, APD-115
C408	Capacitor: fixed, electrolytic, 200 mfd, 20 vdc	M, APD-115
C409	Capacitor: fixed, electrolytic, 200 mfd, 20 vdc	M, APD-115
C501	Capacitor: fixed, electrolytic, 2 mfd, 15 vdc	Y, TE-1149
C502	Capacitor: fixed, electrolytic, 500 mfd, 15 vdc	M, APD-124

TABLE OF REPLACEABLE PARTS

Circuit Ref	Description	Mfr* & Mfr's Designation
C503	Capacitor: fixed, electrolytic, 1 mfd, 15 vdc	Y, TE-1148
R1	Resistor: fixed, metal film, 475 ohms ±1%, ½ w	N, CEC-TO
R2	Resistor: fixed, metal film, 316 ohms ±1%, ½ w	N, CEC-TO
R3	Resistor: fixed, metal film, 68.1 ohms ±1%, ½ w	N, CEC-TO
R4	Resistor: fixed, metal film, 475 ohms ±1%, ½ w	N, CEC-TO
R5	Resistor: fixed, metal film, 316 ohms ±1%, ½ w	N, CEC-TO
R6	Resistor: fixed, metal film, 68.1 ohms ±1%, ½ w	N, CEC-TO
R7	Resistor: fixed, composition, selected value	A
R8	Resistor: fixed, metal film, 24.209 K ±1%, ½ w	N, CEC-TO
R9	Resistor: fixed, metal film, 816.3 ohms ±1%, ½ w	N, CEC-TO
R10	Resistor: fixed, metal film, 3.435 K ±1%, ½ w	N, CEC-TO
R11	Resistor: fixed, metal film, 22 K ±1%, ½ w	N, CEC-TO
R12	Resistor: fixed, metal film, 7.9 K ±1%, ½ w	N, CEC-TO
R13	Resistor: fixed, composition, 390 K ±10%, ½ w	A
R14	Resistor: fixed, composition, 4.7 K ±10%, ½ w	A
R15	Resistor: fixed, composition, 390 K ±10%, ½ w	A
R16	Resistor: fixed, composition, 2.2 K ±5%, ½ w	A
R17	Resistor: fixed, composition, 47 ohms ±10%, ½ w	A
R18	Resistor: fixed, composition, 6.2 K ±5%, ½ w	A
R19	Resistor: fixed, composition, 2.2 K ±5%, ½ w	A
R20	Resistor: fixed, composition, 510 K ±5%, ½ w	A
R21	Resistor: fixed, composition, 2.2 K ±5%, ½ w	A
R22	Resistor: fixed, composition, 270 ohms ±10%, ½ w	A
R23	Resistor: fixed, composition, selected value	A
R24	Resistor: fixed, metal film, 600 ohms ±1%, ½ w	N, CEC-TO
R25	Resistor: fixed, composition, selected value	A
R26	Resistor: fixed, composition, selected value	A
R27	Resistor: fixed, metal film 410.2 ohms ±1%, ½ w	N, CEC-TO
R28	Resistor: fixed, metal film, 129.8 ohms ±1%, ½ w	N, CEC-TO
R29	Resistor: fixed, metal film, 60 ohms ±1%, ½ w	N, CEC-TO
R30	Resistor: fixed, composition, 390 K ±10%, ½ w	A
R31	Resistor: fixed, composition, 2.2 K ±5%, ½ w	A
R32	Resistor: fixed, composition, 18 ohms ±5%, ½ w	A
R33	Resistor: fixed, composition, 510 ohms ±5%, ½ w	A
R34	Resistor: fixed, composition, 390 K ±10%, ½ w	A
R35	Resistor: fixed, composition, 2.2 K ±5%, ½ w	A
R36	Resistor: fixed, composition, 270 ohms ±10%, ½ w	A
R37	Resistor: fixed, metal film, 1.5 K ±1%, ½ w	N, CEC-TO
R38	Resistor: fixed, composition, 200 K ±5%, ½ w	A
R39	Resistor: fixed, composition, 680 ohms ±5%, ½ w	A
R40	Resistor: fixed, composition, 100 ohms ±10%, ½ w	A
R41	Resistor: fixed, composition, 10 K ±10%, ½ w	A
R42	Resistor: fixed, wirewound, 400 ohms ±10%, 10 w	Y, 247E4015
R42A	Resistor: fixed, wirewound, 400 ohms ±10%, 10 w	Y, 247E4015
R43	Resistor: fixed, metal film, 40.2 K ±1%, ½ w	N, CEC-TO
R44	Resistor: fixed, metal film, 40.2 K ±1%, ½ w	N, CEC-TO
R45	Resistor: fixed, metal film, 80.6 K ±1%, ½ w	N, CEC-TO
R46	Resistor: fixed, metal film, 1 K ±1%, ½ w	N, CEC-TO

TABLE OF REPLACEABLE PARTS

Circuit Ref	Description	Mfr* & Mfr's Designation
R101	Resistor: fixed, metal film, 2056.7 ohms ±1%, ½ w	N, CEC-TO
R102	Resistor: fixed, metal film, 1633.7 ohms ±1%, ½ w	N, CEC-TO
R103	Resistor: fixed, metal film, 1297.7 ohms ±1%, ½ w	N, CEC-TO
R104	Resistor: fixed, metal film, 1030.8 ohms ±1%, ½ w	N, CEC-TO
R105	Resistor: fixed, metal film, 818.8 ohms ±1%, ½ w	N, CEC-TO
R106	Resistor: fixed, metal film, 650.4 ohms ±1%, ½ w	N, CEC-TO
R107	Resistor: fixed, metal film, 516.6 ohms ±1%, ½ w	N, CEC-TO
R108	Resistor: fixed, metal film, 410.4 ohms ±1%, ½ w	N, CEC-TO
R109	Resistor: fixed, metal film, 326 ohms ±1%, ½ w	N, CEC-TO
R110	Resistor: fixed, metal film, 258.9 ohms ±1%, ½ w	N, CEC-TO
R111	Resistor: fixed, variable, composition, 500 ohms	E, HML-500
R112	Resistor: fixed, metal film, 649 ohms ±1%, ½ w	N, CEC-TO
R113	Resistor: fixed, composition, selected value	A
R114	Resistor: fixed, composition, 1 meg ±1%, ½ w	A
R115	Resistor: fixed, composition, 180 ojms ±10%, ½ w	A
R116	Resistor: fixed, composition, 4.7 K ±10%, ½ w	A
R117	Resistor: fixed, composition, 270 ohms ±10%, ½ w	A
R118	Resistor: fixed, composition, 47 K ±10%, ½ w	A
R119	Resistor: fixed, composition, 91 K ±5%, ½ w	A
R120	Resistor: fixed, composition, 4.7 K ±10%, ½ w	A
R121	Resistor: fixed, composition, 4.7 K ±10%, ½ w	A
R122	Resistor: fixed, composition, 680 ohms ±5%, ½ w	A
R123	Resistor: fixed, composition, 10 K ±10%, ½ w	A
R124	Resistor: fixed, composition, 10 K ±10%, ½ w	A
R125	Resistor: fixed, composition, 47 K ±10%, ½ w	A
R126	Resistor: fixed, composition, 120 ohms ±10%, ½ w	A
R127	Resistor: fixed, composition, 4.7 K ±10%, ½ w	A
R128	Resistor: fixed, composition, 470 ohms ±5%, ½ w	A
R129	Resistor: fixed, composition, 47 K ±10%, ½ w	A
R130	Resistor: fixed, composition, 47 K ±10%, ½ w	A
R131	Resistor: fixed, composition, 10 K ±10%, ½ w	A
R132	Resistor: fixed, composition, 10 K ±10%, ½ w	A
R133	Resistor: fixed, composition, 47 K ±10%, ½ w	A
R134	Resistor: fixed, composition, 4.7 K ±10%, ½ w	A
R135	Resistor: fixed, composition, 10 K ±10%, ½ w	A
R136	Resistor: fixed, composition, 4.7 K ±10%, ½ w	A
R137	Resistor: fixed, composition, 100 ohms ±10%, ½ w	A
R138	Resistor: fixed, composition, 4.7 K ±10%, ½ w	A
R139	Resistor: fixed, composition, 56 ohms ±5%, ½ w	A
R401	Resistor: fixed, composition, 10 K ±10%, ½ w	A
R402	Resistor: fixed, composition, 10 K ±10%, ½ w	A
R403	Resistor: fixed, composition, 120 ohms ±10%, ½ w	A
R404	Resistor: fixed, composition, 1 K ±10%, ½ w	A
R405	Resistor: fixed, composition, 470 ohms ±5%, ½ w	A
R406	Resistor: fixed, composition, selected value	A
R407	Resistor: fixed, composition, 4.7 K ±10%, ½ w	A
R408	Resistor: fixed, composition, 22 K ±10%, ½ w	A
R409	Resistor: fixed, composition, 10 K ±10%, ½ w	A

TABLE OF REPLACEABLE PARTS

Circuit Ref	Description	Mfr * & Mfr's Designation
R410	Resistor: fixed, composition, 10 K ±10%, ½ w	A
R411	Resistor: fixed, composition, 120 ohms ±10%, ½ w	A
R412	Resistor: fixed, composition, 1 K ±10%, ½ w	A
R413	Resistor: fixed, composition, selected value	A
R414	Resistor: fixed, composition, 470 ohms ±5%, ½ w	A
R415	Resistor: fixed, composition, 4.7 K ±10%, ½ w	A
R416	Resistor: fixed, composition, 22 K ±10%, ½ w	A
R417	Resistor: fixed, composition, 1 K ±10%, ½ w	A
R418	Resistor: fixed, composition, 3.6 K ±5%, ½ w	A
R501	Resistor: fixed, composition, 2.2 K ±5%, ½ w	A
R502	Resistor: fixed, composition, 36 K ±5%, ½ w	A
R503	Resistor: fixed, composition, 1.2 K ±10%, ½ w	A
R504	Resistor: fixed, composition, 4.7 K ±10%, ½ w	A
R505	Resistor: fixed, composition, 10 K ±10%, ½ w	A
R506	Resistor: fixed, composition, 47 K ±10%, ½ w	A
CR1	Diode, silicon	AA, 1N2069
CR2	Diode, zener, 18 volts 10 watts	H, 1N1607
CR101	Diode, germanium	AA, 1N198
CR102	Diode, germanium	AA, 1N198
CR103	Diode, germanium	AA, 1N198
CR104	Diode, germanium	AA, 1N198
CR105	Diode, germanium	AA, 1N198
CR106	Diode, germanium	AA, 1N198
CR107	Diode, germanium	AA, 1N198
CR108	Diode, germanium	AA, 1N198
CR109	Diode, germanium	AA, 1N198
CR110	Diode, germanium	AA, 1N198
CR111	Diode, germanium	AA, 1N198
CR112	Diode, silicon	AA, 1N2069
CR401	Diode, germanium	AA, 1N198
CR402	Diode, silicon	CC, 1N457
CR403	Diode, germanium	AA, 1N198
CR404	Diode, silicon	CC, 1N457
CR405	Diode, zener, 12 volts	CC, 1N759A
CR406	Diode, zener, 9 volts	CC, 1N764
CR501	Diode, germanium	AA, 1N198
CR502	Diode, germanium	AA, 1N198
Q1	Transistor, germanium, PNP	BB, 2N404
Q2	Transistor, germanium, PNP	Y, 2N1748A
Q3	Transistor, germanium, PNP	Y, 2N1748A
Q4	Transistor, germanium, PNP	BB, 2N404
Q5	Transistor, germanium, PNP	Y, 2N1748A
Q6	Transistor, germanium, PNP	Y, 2N1748A
Q7	Transistor, germanium, PNP	BB, 2N404
Q8	Transistor, germanium, PNP	BB, 2N404
Q101	Transistor, germanium, PNP	BB, 2N404
Q102	Transistor, germanium, PNP	BB, 2N404
Q103	Transistor, germanium, PNP	BB, 2N404

TABLE OF REPLACEABLE PARTS

Circuit Ref	Description	Mfr* & Mfr's Designation
Q104	Transistor: germanium, PNP	BB, 2N404
Q105	Transistor: germanium, PNP	BB, 2N404
Q106	Transistor: silicon, NPN	R, 2N2102
Q401	Transistor: germanium, PNP	BB, 2N404
Q402	Transistor: germanium, PNP	BB, 2N404
Q403	Transistor: germanium, PNP	BB, 2N404
Q404	Transistor: germanium, PNP	BB, 2N404
Q405	Transistor: silicon, PNP	M, 2N3638
Q406	Transistor: silicon, PNP	M, 2N3638
Q501	Transistor: silicon, NPN	AA, 2N706
Q502	Transistor: germanium, PNP	BB, 2N404
J1	Jack: (DIAL) for 310 type	Z, 5-J-1329
J2	Jack: (LINE) for 310 type	Z, 5-J-1329
J3	Binding Post: (LINE) tip	K, 29-1R
J4	Binding Post: (LINE) ring	K, 29-1B
J5	Jack: 48 volt, for 310 type	Z, 5-J-1191 CMT
J6	Jack: (MON) for 310 type	Z, M-446A
J7	Binding Post: (EXT WTG) IN	K, 29-1R
J8	Binding Post: (EXT WTG) OUT	K. 29-1R
BP1	Binding Post: sleeve	W, 137-SP
BP2	Binding Post: ground	W, 137-SP
L1	Hold Coil	Q, 1274
L2	Inductor: 7.5 mh	G, 2500-70
L3	Inductor: 2.7 mh	G, 2500-48
L4	Inductor: toroid, 60 mh	V, ET-204-1290-3
L5	Inductor: toroid, 60 mh	V, ET-204-1290-3
T1	Transformer	Q, NES 3345
TH1	Thermistor	J, KA31L1
	Counters: 4 digit	X, TCeZ4E
	Knobs: for rotary switches	O, 648-3L-BB
S1	Switch: rotary, 10 pole, 5 position, INPUT	E, PA1030
S2	Switch: toggle, DPST, TERM/BRDG	C, 81024KB
S3	Switch: toggle, SPST, HOLD	C, 81015K
S4	Switch: rotary, 4 pole, 8 position, MAIN-SENS Attenuator	E, PA1014
S5	Switch: rotary, 4 pole, 4 position, WTG Selector	E, PA1012
S6	Switch: rotary, 2 pole, 11 position, LO LEVEL Attenuator	E, PA1004
S7	Switch: rotary, 2 pole, 11 position, MID LEVEL Attenuator	E, PA1004
S8	Switch: rotary, 2 pole, 11 position, HI LEVEL Attenuator	E, PA1004
	Timer: 1 hour, SPST	T, 71002J
	Knob: for timer	T, K25C1

*See List of Manufacturers Code Letters for Replaceable Parts Table

LIST OF MANUFACTURERS CODE LETTERS FOR TABLE OF REPLACEABLE PARTS

Code Letter	Manufacturer
A	Allen-Bradley Company
B	Amaton Electronic Hardware Company, Inc.
C	Arrow-Hart and Hageman Electric Company
D	Cambridge Thermionic Corporation
E	Centralab
F	Defiance Printed Circuit Corporation
G	Delevan Electronics Corporation
H	Dickson Electronics Corporation
I	Fairchild Semiconductor Division
J	Fenwal Electronics, Inc.
K	Grayhill, Inc.
L	Great Falls Products, Inc.
M	International Electronic Industries
N	IRC, Inc.
O	Kurz-Kasch, Inc.
P	National Radio Company
Q	Northeast Electronics Corporation
R	Radio Corporation of America
S	Raytheon Company
T	M. H. Rhodes, Inc.
U	Sanford Miller Company
V	Sangamo Electric Company
W	Herman H. Smith, Inc.
X	SODECO (Landis and Gyr, Inc.)
Z	Switchcraft, Inc.
AA	Sylvania Electric Products, Inc.
BB	Texas Instruments, Inc.
CC	Transitron Electronic Corporation

APPENDIX A

MODEL TTS 58ARP POWER SUPPLY

1.0 GENERAL

1.01 The TTS 58ARP Power Supply is located to the right of the TTS 58ARP main unit on the same 19" panel.

1.02 The power supply unit is designed to supply the TTS 58ARP 18 volts DC from a 115 volt AC source in conjunction with the existing regulator circuit in the TTS 58ARP.

2.0 PERFORMANCE DATA

2.01 The TTS 58ARP Power Supply will operate from 47 Hz to 63 Hz single phase commercial AC power at 115 volts AC ±10%.

2.02 Maximum current drain from the power supply is 90 ma DC.

3.0 CIRCUIT DESCRIPTION

3.01 The 115 volt AC source is stepped down to 28 volts AC by T1 and is rectified by a full wave rectifier CR1, CR2, CR3, CR4. (See Figure 1, Appendix A.)

3.02 Filtering is accomplished by an RC pi network, C1, C2, and R1.

3.03 Regulation utilizes the 18 volt zener CR2 that is located near Amplifier 2. (See Figure 11.)

3.04 Relay K1 controls the DC lamp, LP2.

4.0 CONTROLS AND TERMINALS

4.01 POWER Switch

a. The POWER switch, S1, controls only the AC power supply. The AC lamp indicates when S1 is closed.

b. The DC lamp indicates that 18 volts is connected to the TTS 58ARP circuit via the AC power supply.

4.02 Terminals

a. TB1 is located above the AC cord on the rear of the power supply.

b. 18 volts DC will appear at terminals 1 and 2 of TB1 when the POWER switch is turned on. These terminals should only be used as test points.

5.0 CALIBRATION

5.01 The TTS 58ARP does not require calibration.

6.0 OPERATION

6.01 See Section 4.0, page 4.1 of manual.

7.0 MAINTENANCE

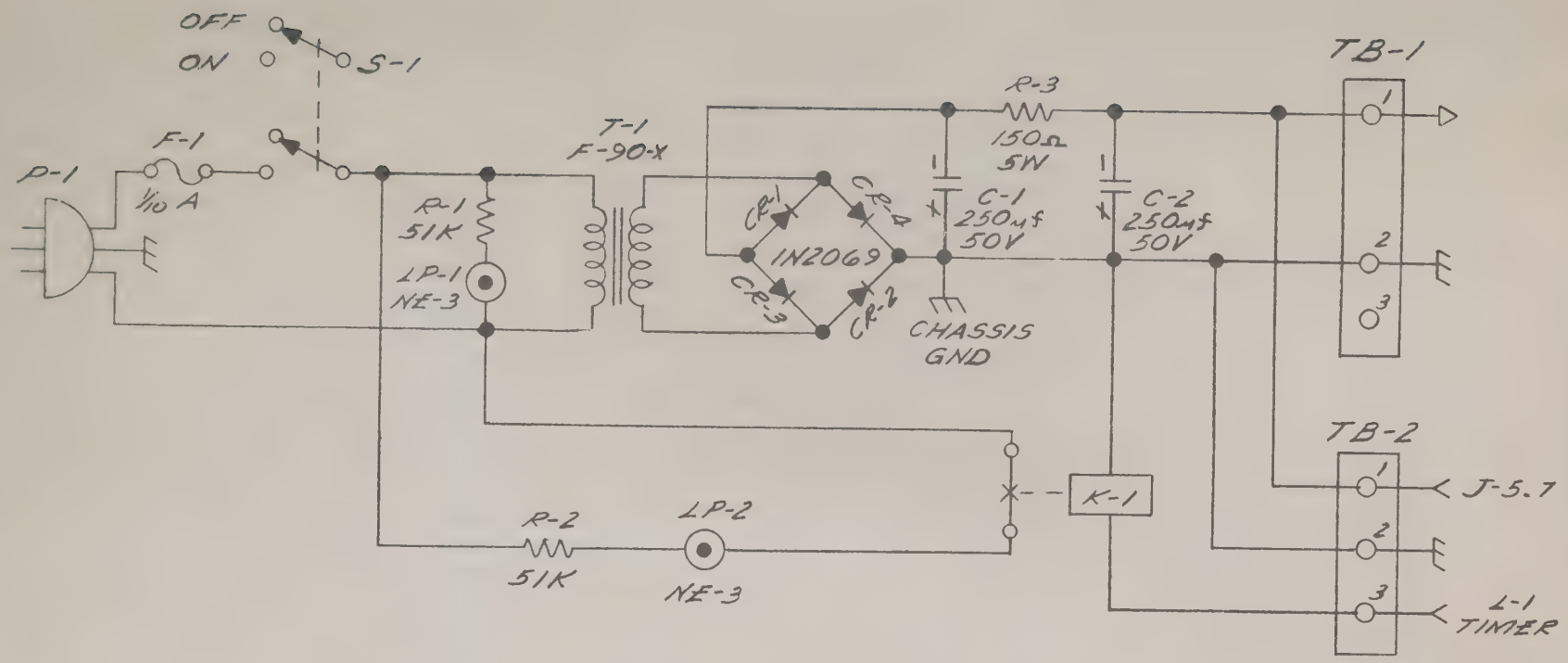
7.01 The TTS 58ARP does not require routine maintenance.

7.02 In the event of a malfunction, it should be insured that:

a. The fuse is not blown.

b. The malfunction is in the AC power supply. This can be checked by operating the set from a 48 volt source. See paragraph 4.11 of manual.

c. The 115 volt AC source is, in fact, present at the AC line being used.



MODEL TTS-58ARP
POWER SUPPLY

FIG. 1

TABLE OF REPLACEABLE PARTS FOR MODEL TTS 58ARP POWER SUPPLY

Circuit Ref	Description	Mfr & Mfr's Designation
C1	Capacitor: fixed, electrolytic, 250 mfd, 50 vdc	H, TVA-1312
C2	Capacitor: fixed, electrolytic, 250 mfd, 50 vdc	H, TVA-1312
R1	Resistor: fixed, wirewound, 150 ohms ±5%, 5 w	H, 243E1515
R2	Resistor: fixed, composition, 51 K ±5%, ½ w	A
R3	Resistor: fixed, composition, 51 K ±5%, ½ w	A
CR1	Diode: silicon	I, 1N2069
CR2	Diode: silicon	I, 1N2069
CR3	Diode: silicon	I, 1N2069
CR4	Diode: silicon	I, 1N2069
K1	Relay	G, S5D
T1	Transformer: Power	U, F-90X
F1	Fuse Holder	C, HKP
F1	Fuse	C, MDL-1/10
DS1	Lamp Assembly	D, 1054428722
	Lamp: neon	E, NE-3
DS2	Lamp Assembly	D, 1054428722
	Lamp: neon	E, NE-3
S1	Switch: toggle, DPST, POWER	F, D-81024KB
P1	Plug: male	F, 7593
	AC Line Cord Plug: female	F, 7595
	AC Line Cord: 3-wire	B, 17236

LIST OF MANUFACTURERS CODE LETTERS

Code Letter	Manufacturer
A	Allen-Bradley Company
B	Belden Manufacturing Company
C	Bussman Manufacturing
D	Dialight Corporation
E	General Electric Company
F	Harvey Hubbell, Inc.
G	Potter and Brumfield
H	Sprague Electric Company
I	Switchcraft, Inc.
J	Triad Distributor

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